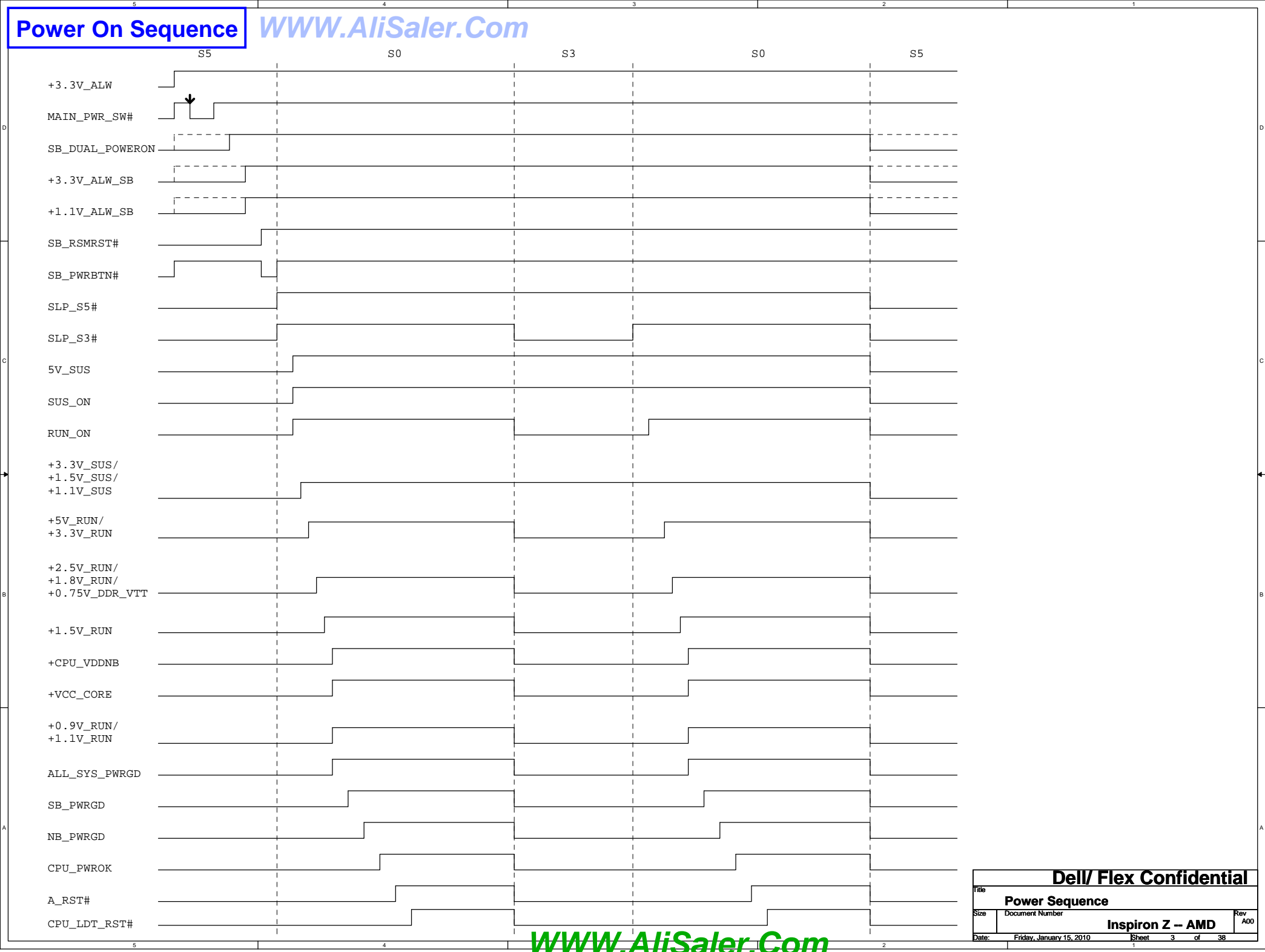


Power States						
Power Rail	Control Signal	S0	S3	S4	S5/ AC-In	G3/ Battery Only
+PWR_SRC	N/A	V	V	V	V	V
+0.75V_DDR_VTT	RUN_ON	V				
+0.9V_RUN	RUN_ON	V				
+1.1V_ALW_SB	SB_DUAL_PWRON	V	V	V	V	
+1.1V_SUS	SUS_ON	V	V			
+1.1V_RUN	RUN_ON	V				
+1.5V_SUS	SUS_ON	V	V			
+1.5V_RUN	RUN_ON	V				
+1.8V_RUN	RUN_ON	V				
+2.5V_RUN	RUN_ON	V				
+3.3V_ALW	+3.3V_EN2	V	V	V	V	V
+3.3V_ALW_SB	SB_DUAL_PWRON	V	V	V	V	
+3.3V_SUS	SUS_ON	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_KBVCC	N/A	V	V	V	V	V
+5V_LDO	N/A	V	V	V	V	V
+5V_SUS	5V_SUS_ON	V	V			
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	N/A	V	V	V	V	V
+LCDVCC	LCD_DIGON	V				
+CPU_VDDNB	2.5V_PWRGD	V				
+VCC_CORE	2.5V_PWRGD	V				
+RTC_CELL	N/A	V	V	V	V	V
+USB_RIGHT_PWR	USB_EN#	V	V			
+USB_LEFT_PWR	USB_EN#	V	V			

Power On Sequence

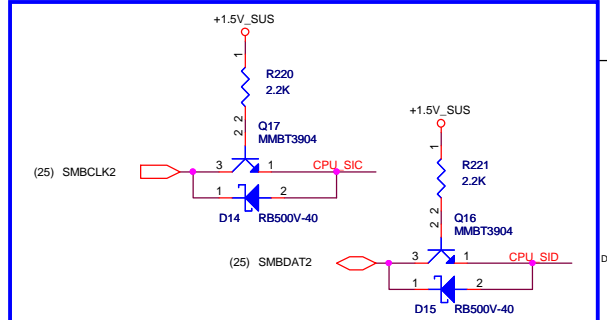
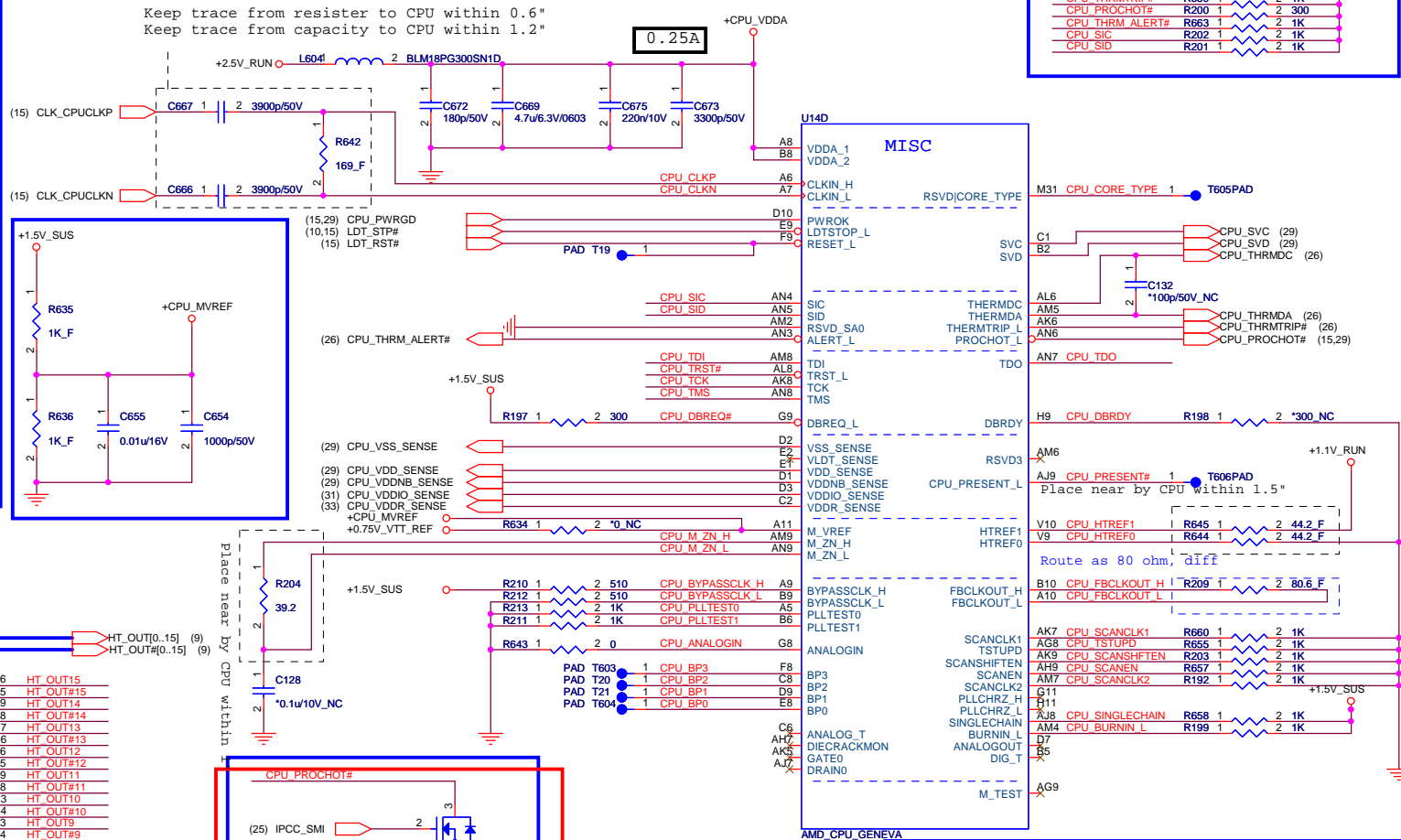
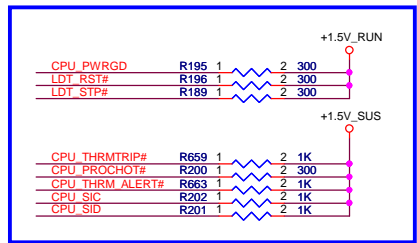
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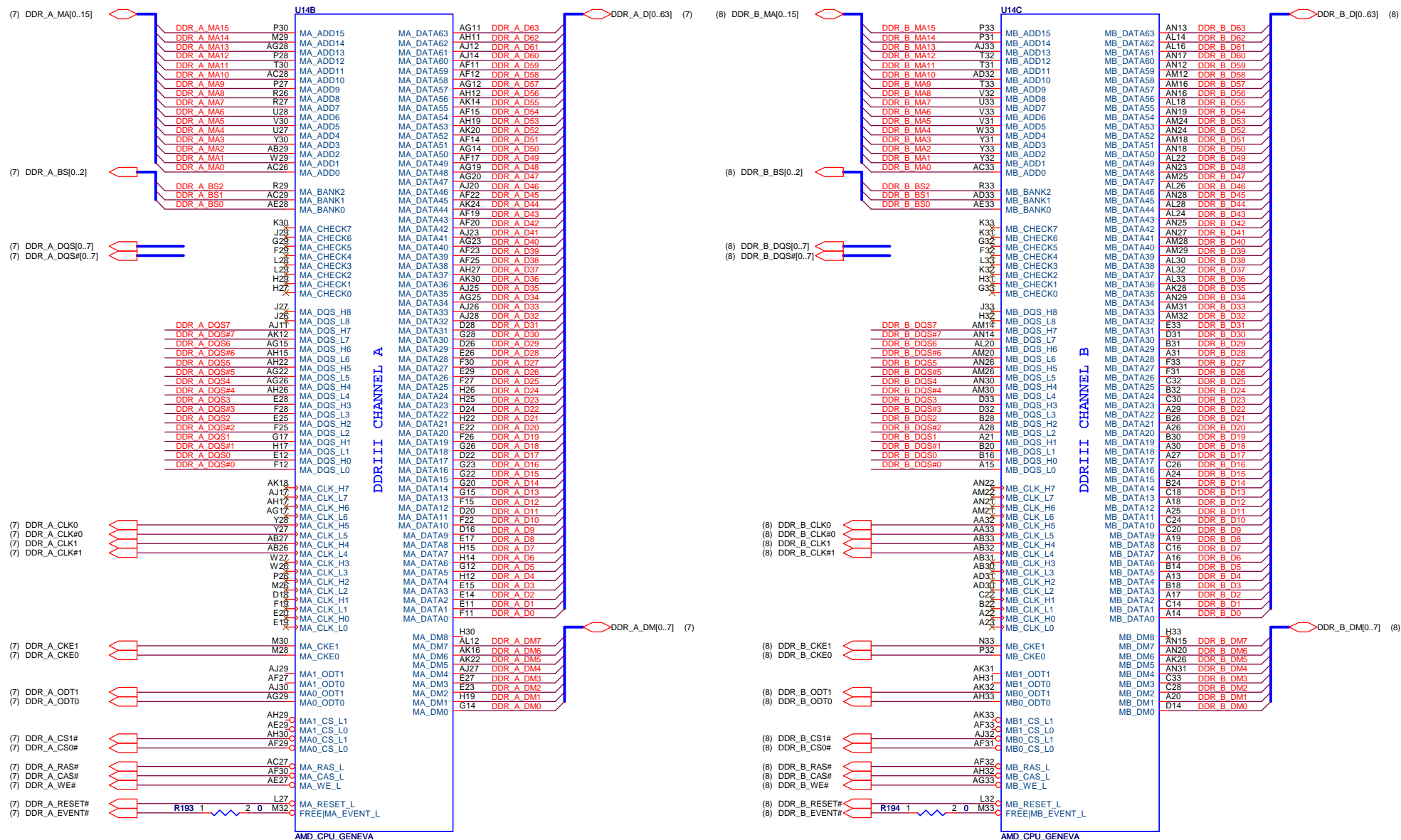
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Signal Name		Type Struct ¹	Header	Termination	Level Shift ²	Termin. Voltage
EST2	DRAIN0	-	Unconnected	-	-	-
EST3	GATE0	-	Unconnected	-	-	-
EST6	DIECRACKMON		Unconnected			
EST7	ANALOG_I		Unconnected			
EST8	DIG_I	-	Unconnected	-	-	-
EST9	ANALOGIN			Tie to VSS		
EST10	ANALOGOUT		Unconnected			
EST14	BP0	O P/P	BP, Pin 1 or TP	-		-
EST15	BP1	O P/P	BP, Pin 3 or TP	-		-
EST16	BP2	O P/P	BP, Pin 5 or TP	-		-
EST17	BP3	O P/P	BP, Pin 7 or TP	-		-
EST18	PLLTEST1		SCAN, pin 7 and HDT+, pin 20	1 K Ω		VSS
EST19	PLLTEST0		SCAN, pin 9 and HDT+, pin 18	1 K Ω		VSS
EST20	SCANCLK2	I	SCAN, pin 19	1 K Ω		VSS
EST21	SCANEN	I	SCAN, pin 11	1 K Ω		VSS
EST22	SCANSHIFTEN	I	SCAN, pin 13	1 K Ω		VSS
EST23	TSTUPD		TP	1 K Ω		VSS
EST24	SCANCLK1	I	SCAN, pin 17	1 K Ω		VSS
EST25_H	BYPASSCLK_H	I	TP	510 Ω		VDDIO
EST25_L	BYPASSCLK_L	I	TP	510 Ω		VSS
EST26	BURNIN_L	-	Termination only	1 K Ω		VDDIO
EST27	SINGLECHAIN	I		1 K Ω		VDDIO
EST28_H	H_FLCLKRZ_P		Unconnected			
EST28_L	L_FLCLKRZ_N		Unconnected			
EST29_H	H_FBCCLKOUT_P			80.6 Ω (differential)		
EST29_L	L_FBCCLKOUT_N					

DELH-40GAB4900-X000	Athlon Single Core 1.7G AMK125DBV13GM	DELH-11D0020000003G IC CPU AMK125DBV13GM 1G7 BGA-812
DELH-40GAB4900-X001	Athlon Dual Core 1.3G AMK325DBV23GM	DELH-11D0020000002G IC CPU AMK325DBV23GM 1G3 BGA-812
DELH-40GAB4900-X002	Turion Dual Core 1.5G TMK625DBV23GM	DELH-11D0020000001G IC CPU TMK625DBV23GM 1G5 BGA-812

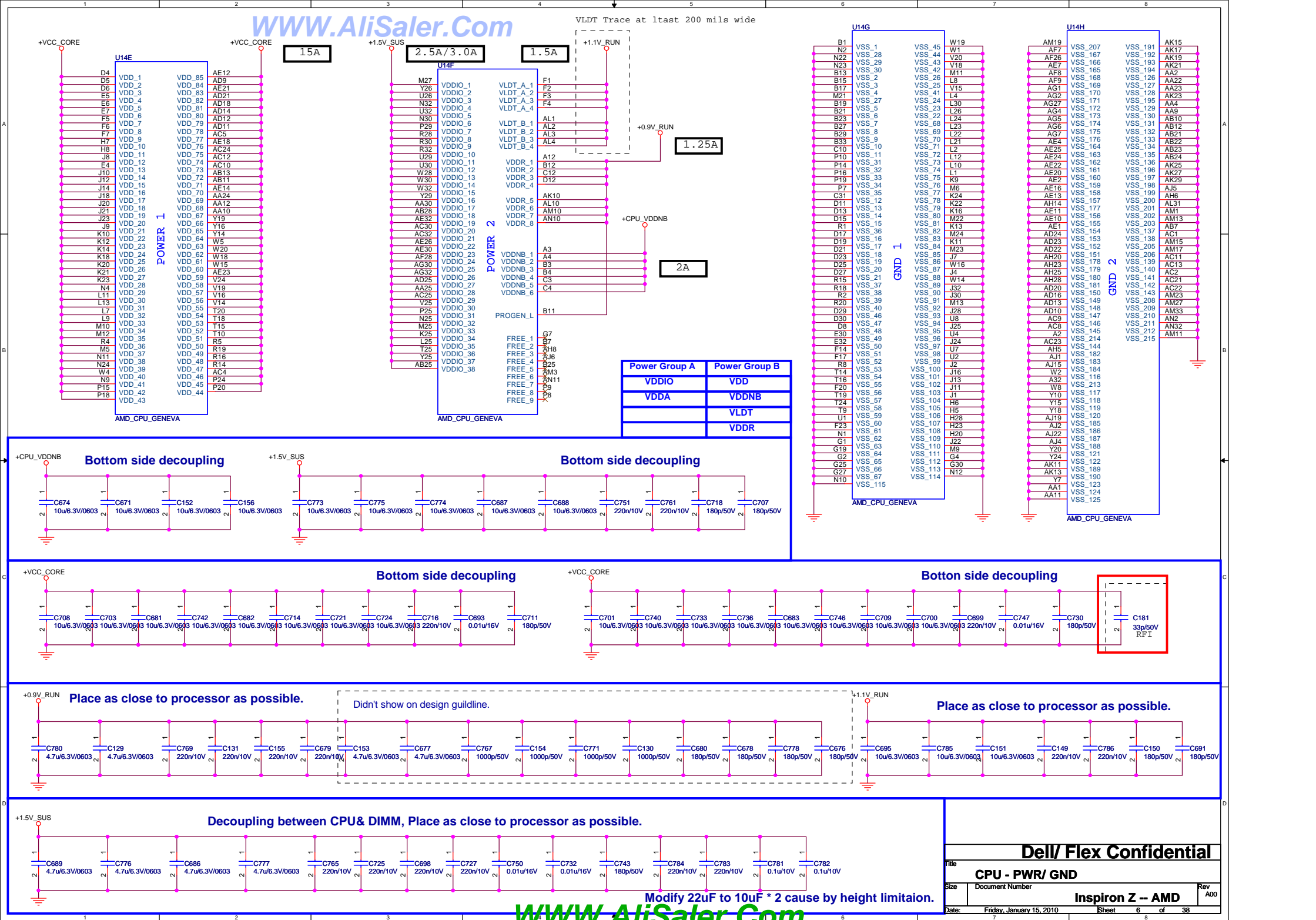


Title				
CPU - HT/ MISC				
Size	Document Number			Rev
	Inspiron Z -- AMD			A00
Date:	Friday, January 15, 2010	Sheet	4	of 38

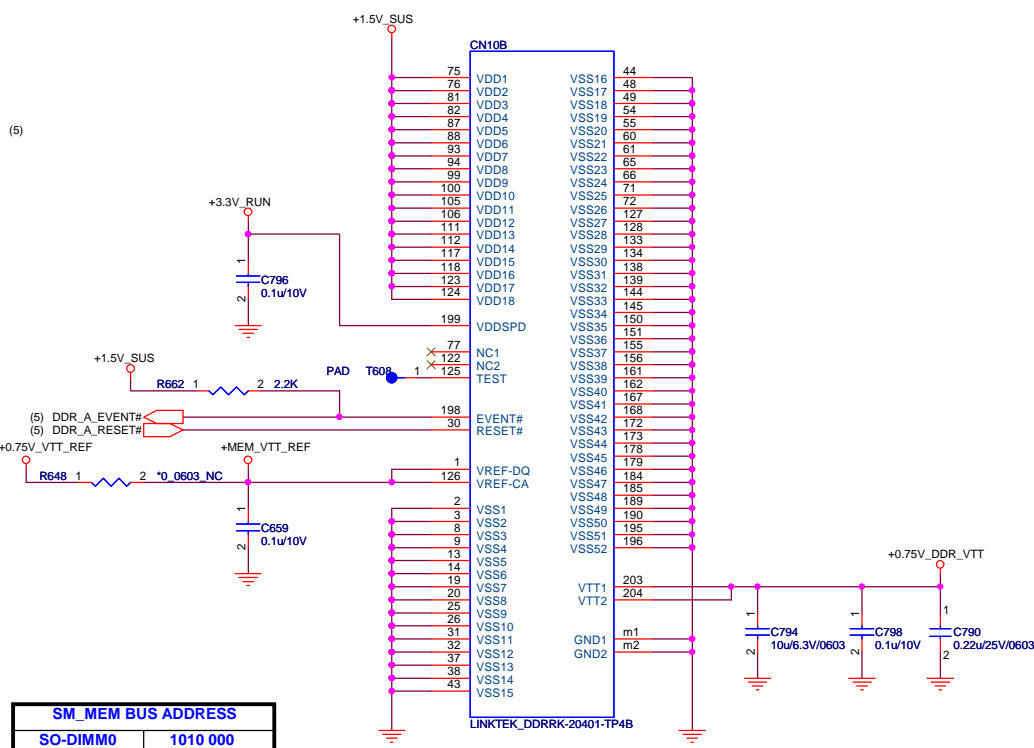
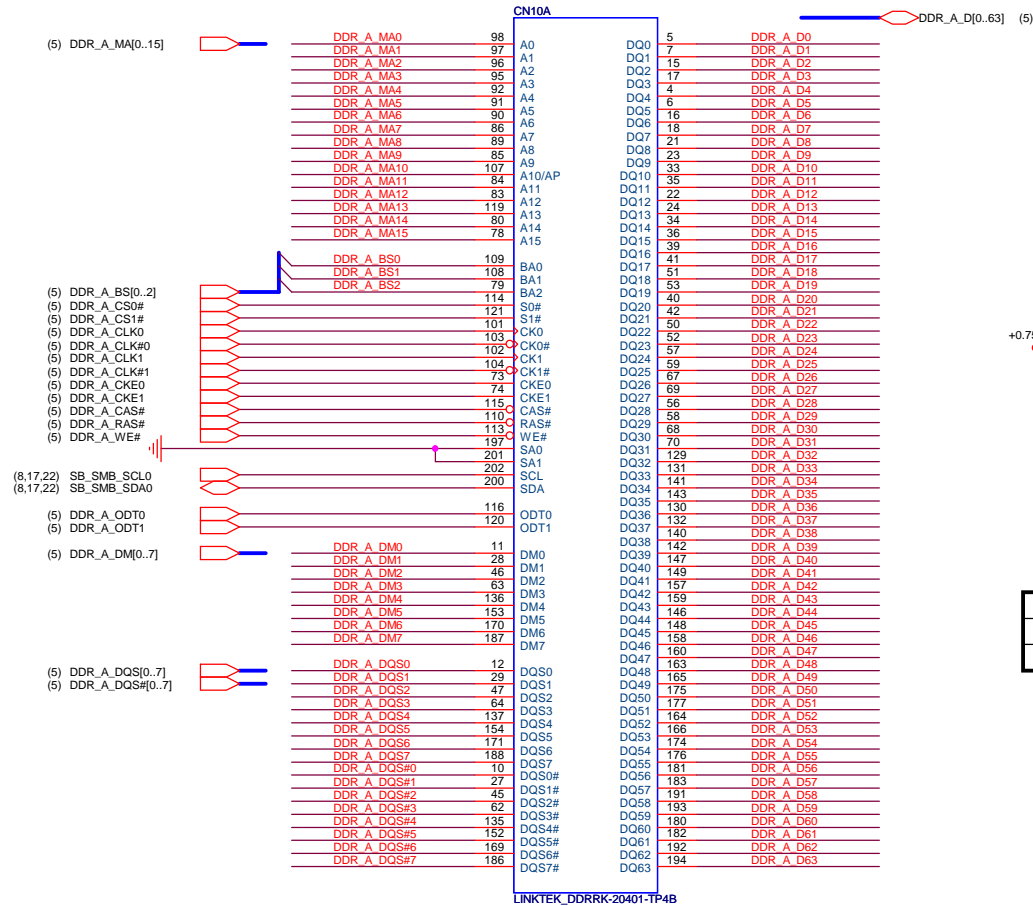


Dell/ Flex Confidential

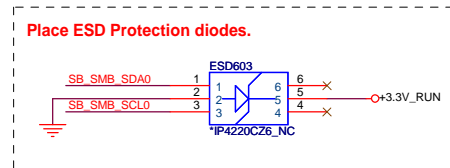
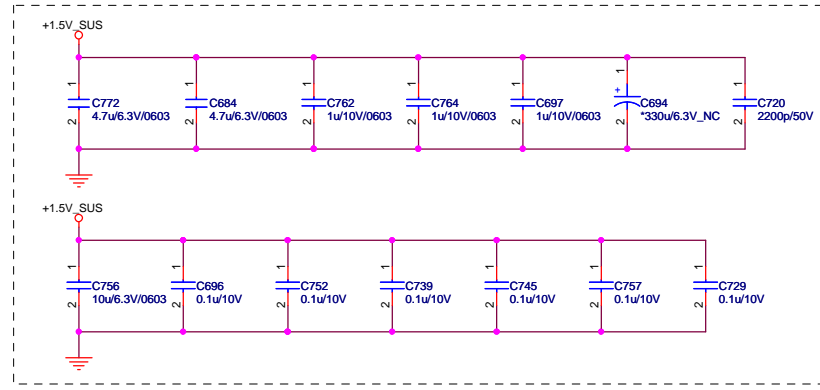
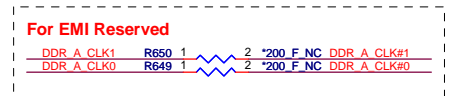
Title			
CPU - DDR I/F			
Size	Document Number	Inspiron Z -- AMD	Rev A00
Date:	Friday, January 15, 2010	Sheet	5 of 38

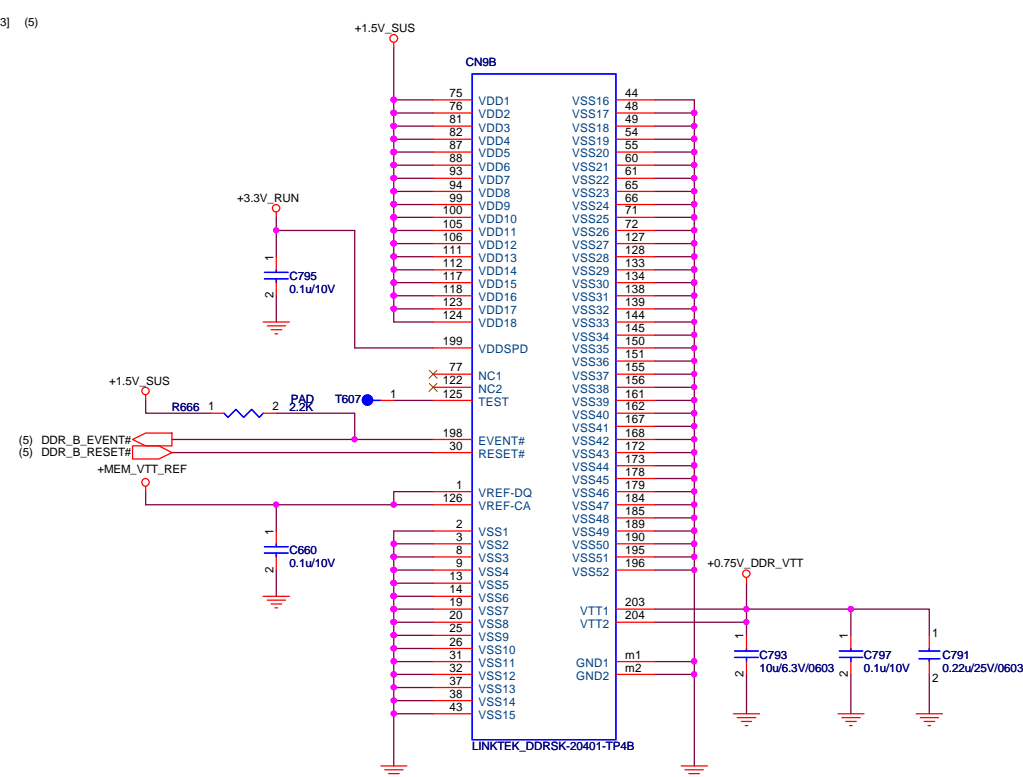


DDR3 DIMM A



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001





The diagram shows a voltage regulator circuit. The input is labeled $+1.5V_{SUS}$. A resistor $R652$ (1K_F) is connected between the input and a node. This node is connected to the non-inverting input of an op-amp (pin 1). The op-amp's output (pin 2) is connected to a node that is also connected to a resistor $R651$ (1K_F) and a capacitor $C763$ (0.01uF/16V). The other end of $R651$ and $C763$ is connected to ground. The output of the op-amp is labeled $+MEM_VTT_REF$. A capacitor $C758$ (1000pF/50V) is connected between the output and ground.

(4) HT_OUT[0..15]
(4) HT_OUT#0..15

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HT_IN[0..15] (4)
HT_IN#0..15 (4)

NB HT/ PCIE

HT_OUT0 Y25
HT_OUT#0 Y24
HT_OUT1 V22
HT_OUT#1 V23
HT_OUT2 V25
HT_OUT#2 V24
HT_OUT3 U24
HT_OUT#3 U25
HT_OUT4 Y25
HT_OUT#4 T24
HT_OUT5 P22
HT_OUT#5 P23
HT_OUT6 P25
HT_OUT#6 P24
HT_OUT7 N24
HT_OUT#7 N25
HT_OUT8 AC24
HT_OUT#8 AC25
HT_OUT9 AB25
HT_OUT#9 AB24
HT_OUT10 AA24
HT_OUT#10 AA25
HT_OUT11 Y22
HT_OUT#11 Y23
HT_OUT12 W21
HT_OUT#12 W20
HT_OUT13 V21
HT_OUT#13 V20
HT_OUT14 U20
HT_OUT#14 U21
HT_OUT15 U19
HT_OUT#15 U18

PART 1 OF 6

HT_TXCAD0P D24
HT_TXCAD0N D25
HT_TXCAD1P E24
HT_TXCAD1N E25
HT_TXCAD2P F25
HT_TXCAD2N F23
HT_TXCAD3P F22
HT_TXCAD3N H23
HT_TXCAD4P H22
HT_TXCAD4N J25
HT_TXCAD5P J24
HT_TXCAD5N K24
HT_TXCAD6P K25
HT_TXCAD6N K23
HT_TXCAD7P K22
HT_TXCAD7N F21
HT_TXCAD8P G21
HT_TXCAD8N G20
HT_TXCAD9P J20
HT_TXCAD9N J21
HT_TXCAD10P J18
HT_TXCAD10N K17
HT_TXCAD11P L19
HT_TXCAD11N J19
HT_TXCAD12P M19
HT_TXCAD12N L18
HT_TXCAD13P M21
HT_TXCAD13N P21
HT_TXCAD14P P19
HT_TXCAD14N M18
HT_TXCAD15P M18
HT_TXCAD15N

HT_RXCLK0P T22
HT_RXCLK0N T23
HT_RXCLK1P AB23
HT_RXCLK1N AA22
HT_RXCTL0P M22
HT_RXCTL0N M23
HT_RXCTL1P R21
HT_RXCTL1N R20
HT_RXCALP C23
HT_RXCALN A24

HT_TXCLK0P H24
HT_TXCLK0N H25
HT_TXCLK1P L21
HT_TXCLK1N L20
HT_TXCTL0P M24
HT_TXCTL0N M25
HT_TXCTL1P P19
HT_TXCTL1N R18
HT_TXCALP B24
HT_TXCALN B25

HT_CLKIN0 (4)
HT_CLKIN#0 (4)
HT_CLKIN1 (4)
HT_CLKIN#1 (4)
HT_CTLIN0 (4)
HT_CTLIN#0 (4)
HT_CTLIN1 (4)
HT_CTLIN#1 (4)
HT_INCAL (4)
HT_INCAL# (4)

HYPER TRANSPORT CPU
I/F

HT_OUTCAL# A24
HT_OUTCAL 301 F

HT_INCAL# B25
HT_INCAL 2 301 F

ATL_RS880M

PART 2 OF 6

PCIE I/F
GFX

GFX_RX0P D4
GFX_RX0N A4
GFX_RX1P B3
GFX_RX1N C2
GFX_RX2P C1
GFX_RX2N E5
GFX_RX3P F5
GFX_RX3N G5
GFX_RX4P G6
GFX_RX4N H5
GFX_RX5P H6
GFX_RX5N J6
GFX_RX6P J7
GFX_RX6N J8
GFX_RX7P L5
GFX_RX7N L6
GFX_RX8P L8
GFX_RX8N M7
GFX_RX9P M8
GFX_RX9N P7
GFX_RX10P M7
GFX_RX10N P5
GFX_RX11P M5
GFX_RX11N P8
GFX_RX12P R6
GFX_RX12N R5
GFX_RX13P R4
GFX_RX13N P3
GFX_RX14P T4
GFX_RX14N T3
GFX_RX15P T2
GFX_RX15N

HDMI_TX2_P_C A5
HDMI_TX2_N_C B5
HDMI_TX1_P_C B4
HDMI_TX1_N_C C3
HDMI_TX0_P_C B2
HDMI_TX0_N_C D1
HDMI_CLK_P_C E2
HDMI_CLK_N_C E2
DP_LANE0_P_C E1
DP_LANE0_N_C F4
DP_LANE1_P_C F3
DP_LANE1_N_C F1
DP_LANE2_P_C F2
DP_LANE2_N_C H4
DP_LANE3_P_C H3
DP_LANE3_N_C H1
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NB LVDS/ PM

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110mA	+3.3V_RUN
20mA	+1.8V_RUN
4mA	CRT disable

PART 3 OF 6

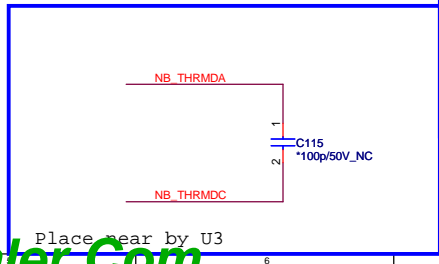
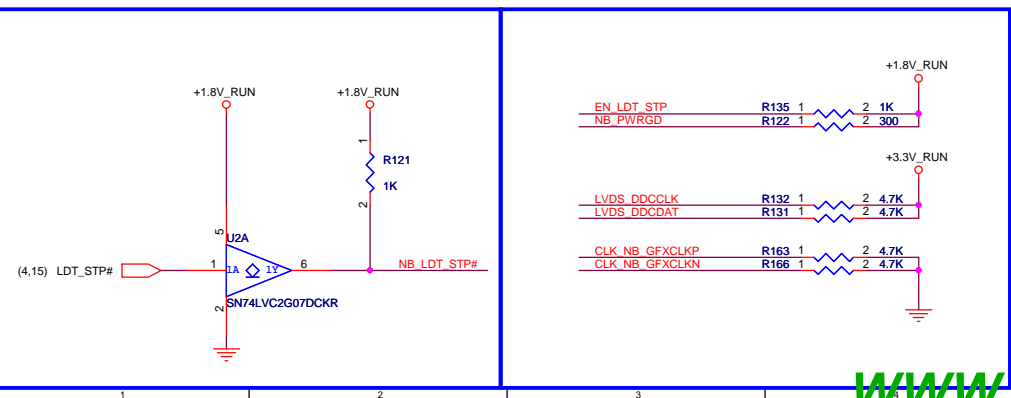
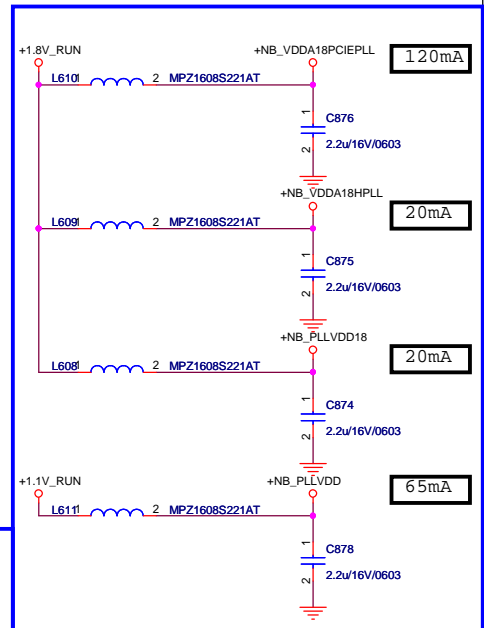
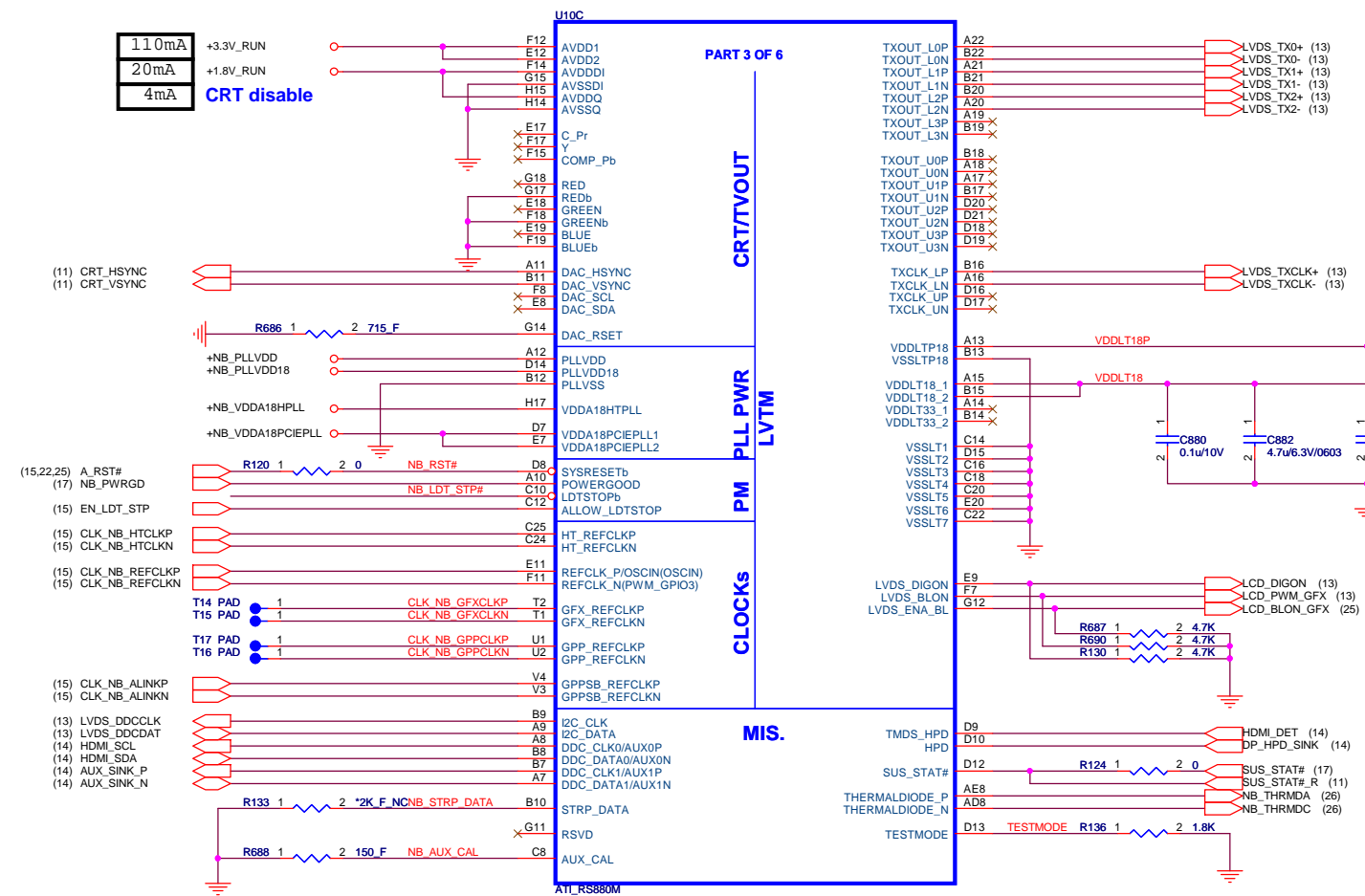
CRT/VOUT

PLL PWR

PM

CLOCKS

MIS.



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Title: NB - LVDS/ CRT/ PM

Size: Document Number

Date: Friday, January 15, 2010

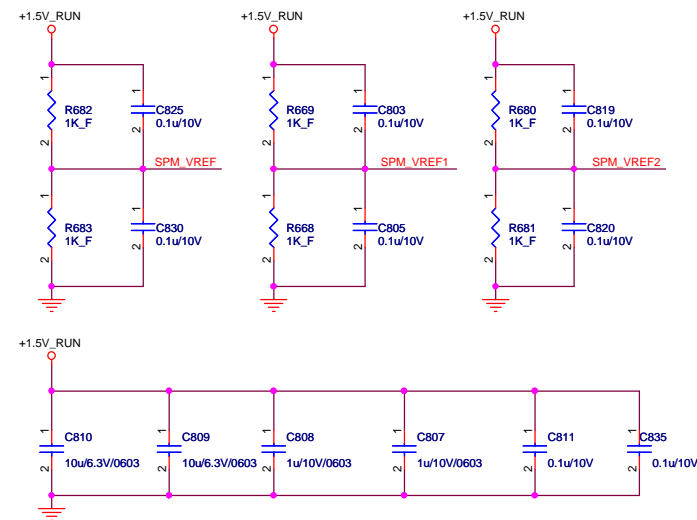
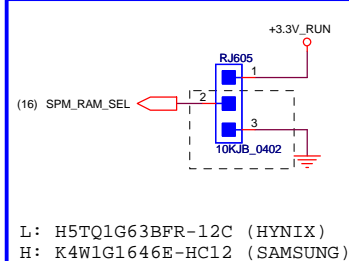
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Inspiron Z -- AMD

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RS880M H/W STRAPS

STRAP_DEBUG_BUS_GPIO_ENABLEb

1 = Disable
0 = Enable



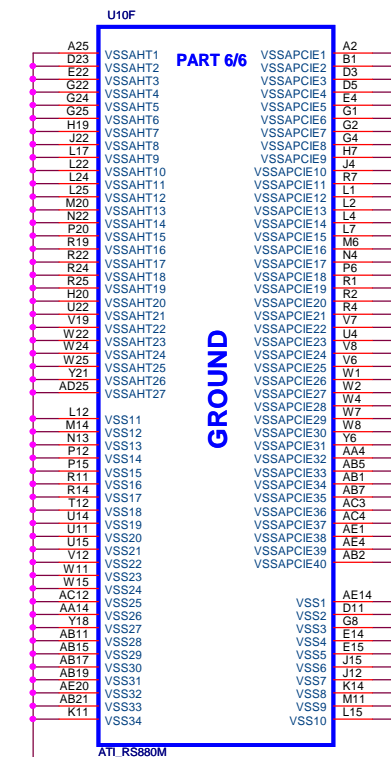
DFT GPIO1: LOAD EEPROM STRAPS

connected, or use default values if not connected



RS880: Enable Side Port Memory

```
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

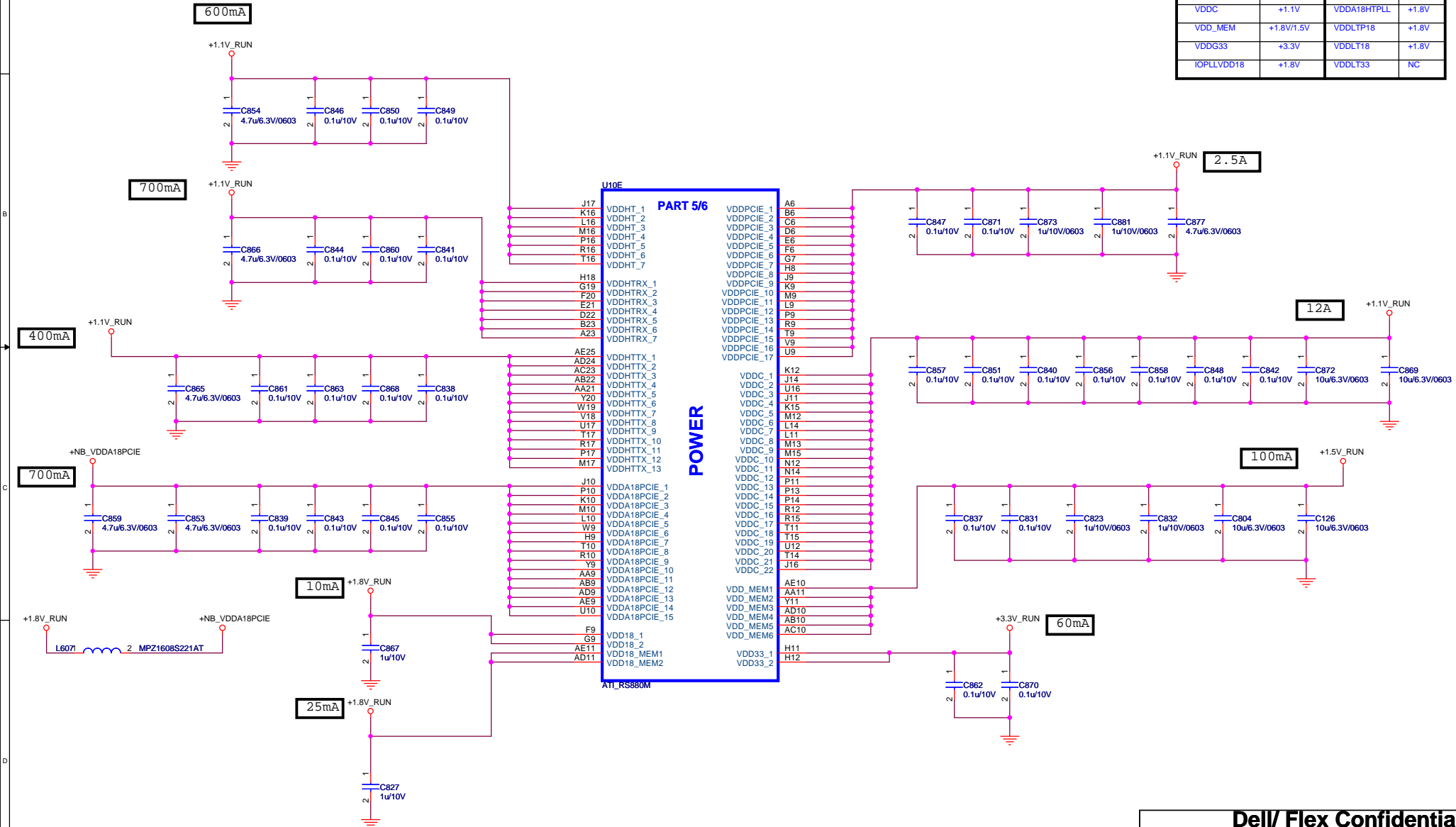


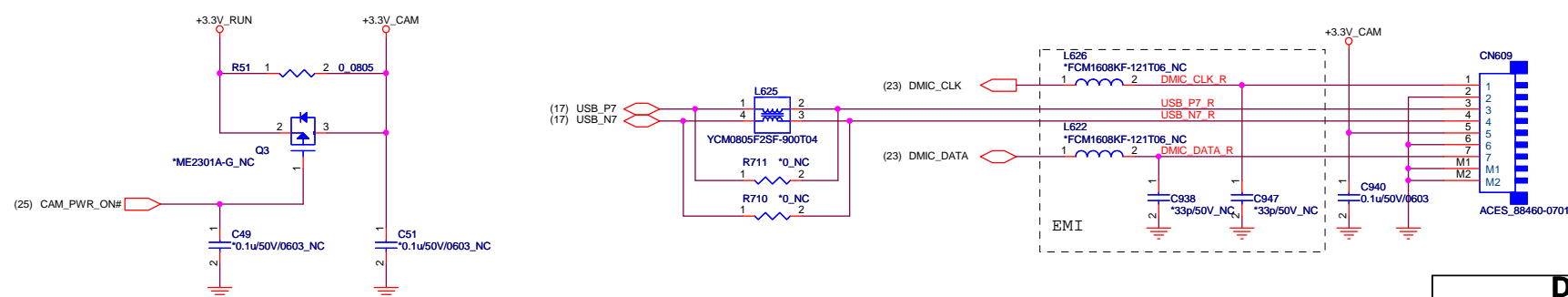
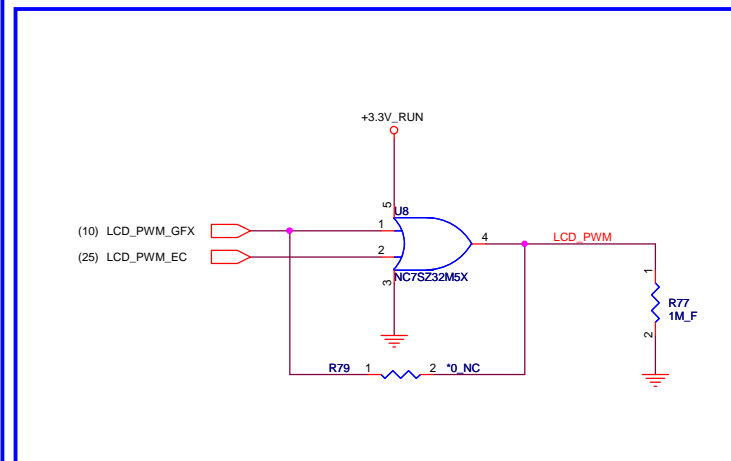
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Title			
NB - STRAP/ SIDE PORT			
Size	Document Number		Rev A00
	Inspiron Z -- AMD		
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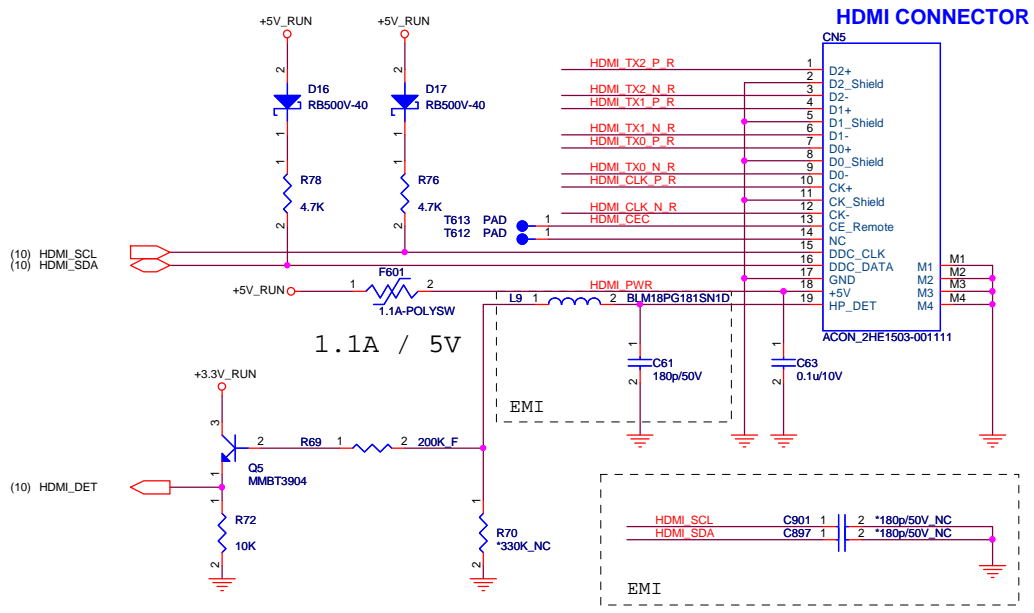
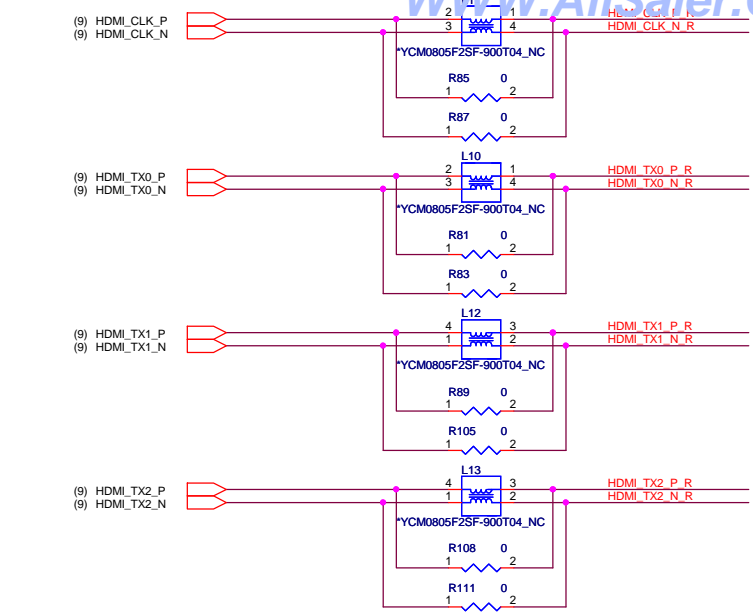
RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVDD18	+1.8V	VDDL18	NC

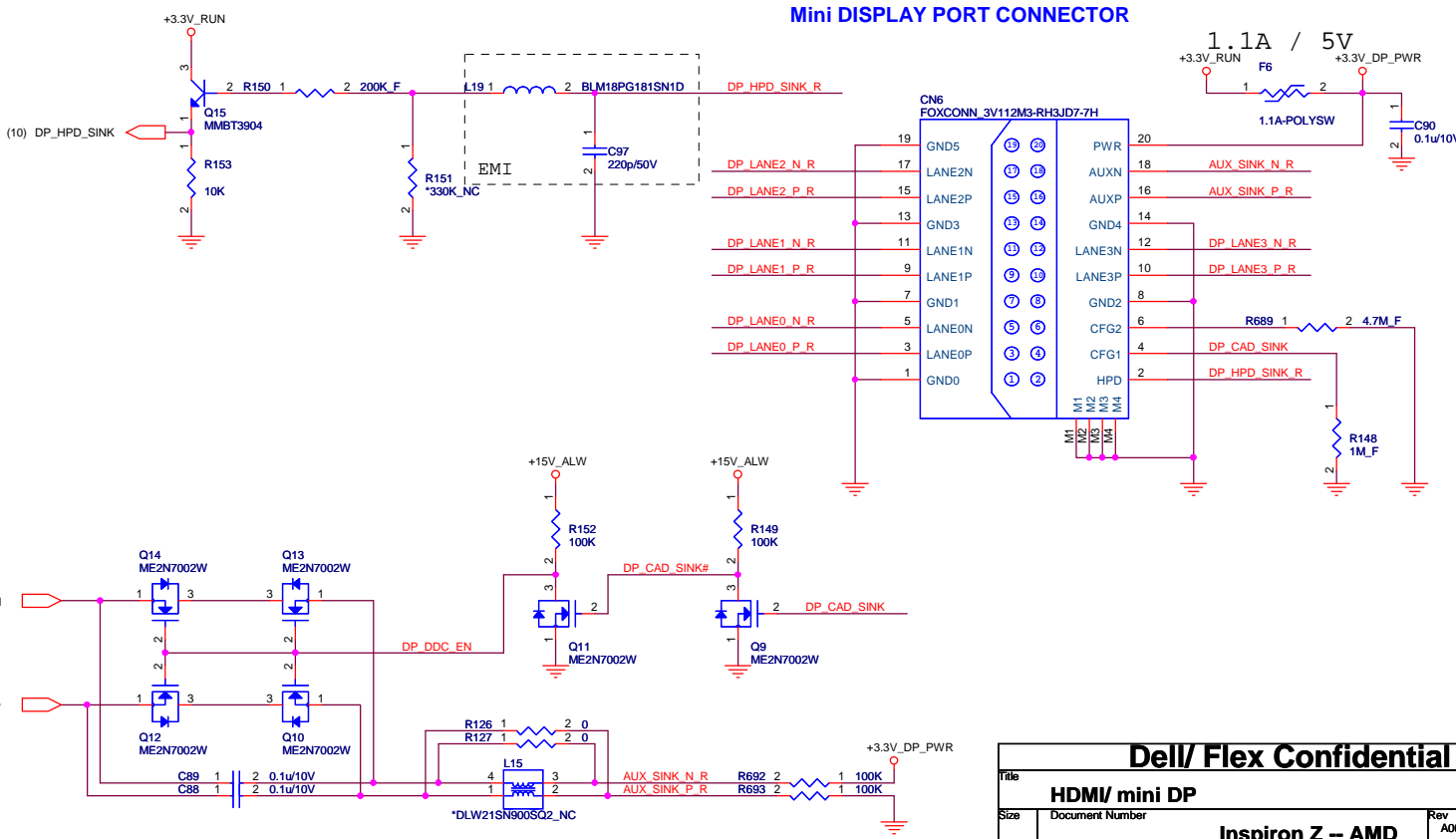
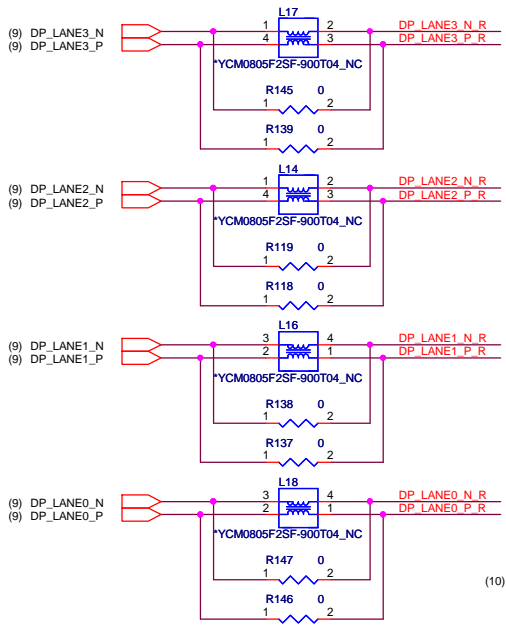




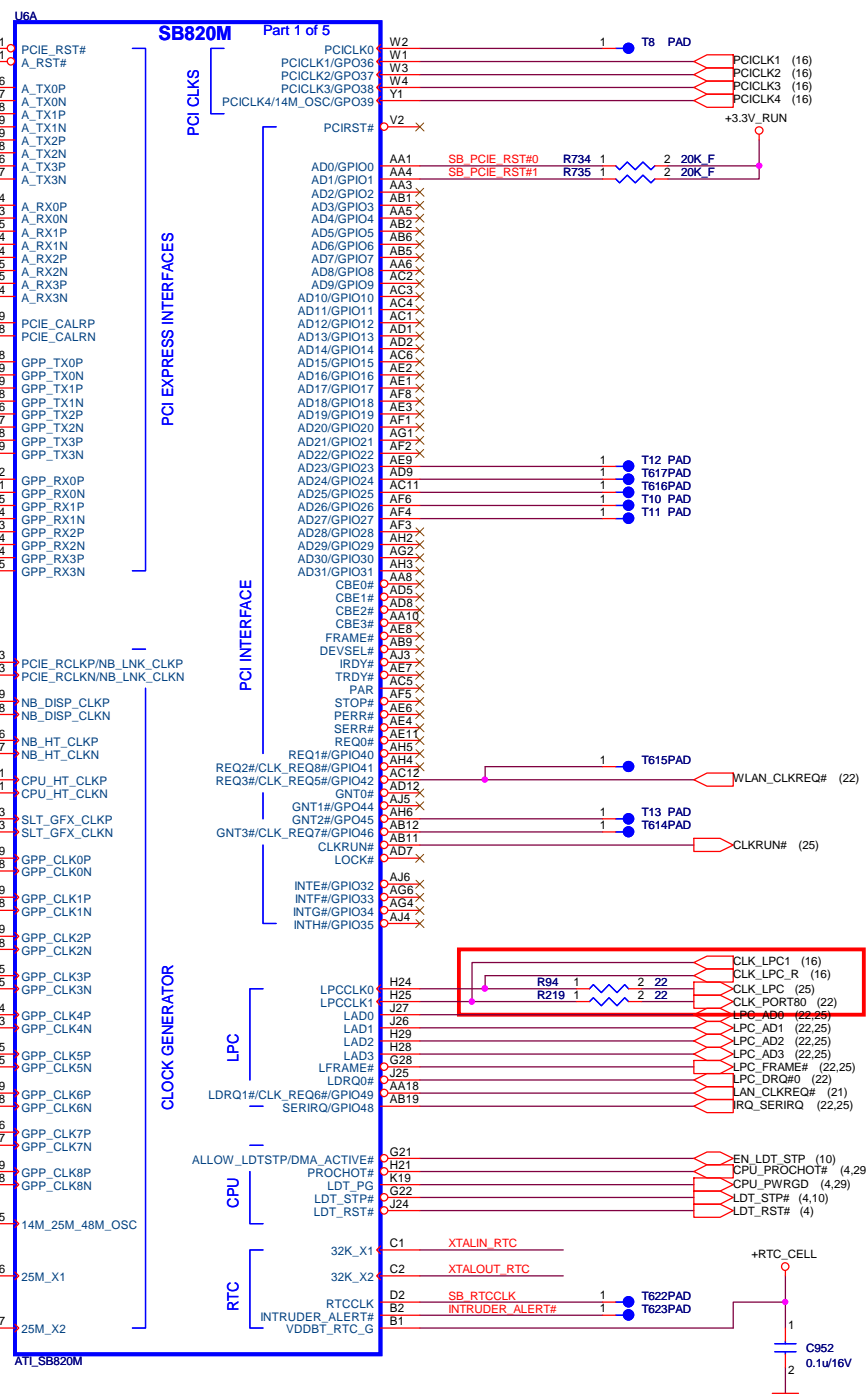
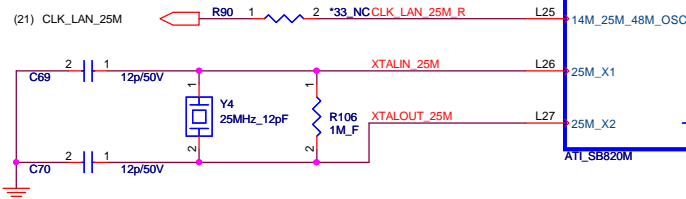
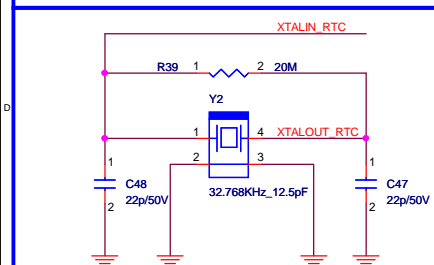
Reserve For EMI



Reserve For EMI



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Title			
HDMI/ mini DP			
Size			
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A00			
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SB820M H/W STRAPS

Type I are captured on RSMRST#
Type II are captured on PWRGD.

ECEnableStrap (LPCCLK0)

Embedded Controller (EC):

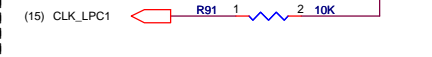
L: Disable
H: Enable



CLKGEN (LPCCLK1)

Define Clock Generator:

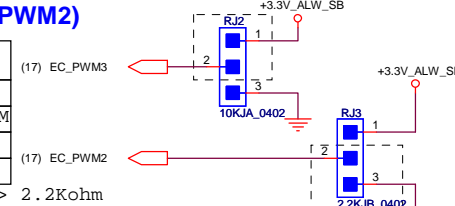
L: External clock mode
H: Internal clock mode



ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1	ROMTYPE_0	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

Pull-High --> 10Kohm, Pull-Low --> 2.2Kohm



BIF_GEN2_COMPLIANCE_Strap (PCI CLK1)

Set PCIe to Gen II mode:

SB820M: Only provision for Pull down is required, not install by default.



BootFailTmrEn (PCI CLK2)

Watchdog function:

L: Disable BootFailtmr function
H: Enable BootFailtmr function



DefaultStrapMode (PCI CLK3)

Default Debug Straps:

L: Disable Debug Straps
H: Select external Debug Straps



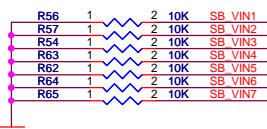
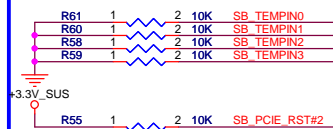
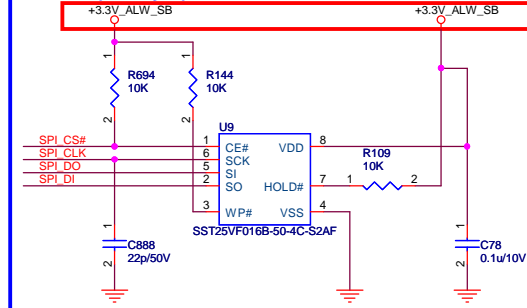
CPUClkSel (PCI CLK4)

CPU/ NB HT Clock Selection:

L: Reserved
H: Required setting for integrated clock mode



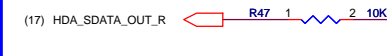
16Mbit (2M Byte), SPI



CoreSpeedMode (AZ_SDOUT)

Slow down core clock for low power mobile platform:

L: Performance Mode
H: Low Power Mode



Type I : LPCCLK0, EC_PWM3& EC_PWM2
Type II : the rest of strapping

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SB - SATA/ SPI/ STAP		
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SB820M Debug Straps

PciPIIByp (PCI AD27)

Bypass PCI PLL
(Used in functional test at tester):

L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK
(Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable

L: ILA Auto run enable
H: ILA Auto run disable
(Internal Pull-Up of 15Kohm)

FCClkByP (PCI AD25)

Bypass FC CLK

L: Bypass internal FC CLK
(Used in functional test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

I2C ROM Enable. Load the setting for A-Link Express/ PLL/ music control from I2C ROM

L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Bootting from PCI memory

L: Route ROM fetch tp PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/ PCI_GNT3)

PCIe EEPROM Data/ Clock

Connected to PCIe EEPROM SDA/ SCL pin or provided test point access for lad use.

SERIAL ATA

HW MONITOR

SPI ROM

FLASH

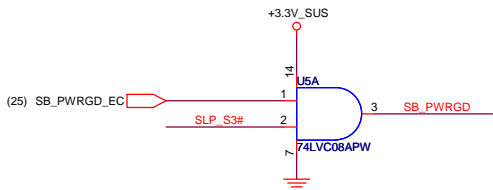
SERIAL ATA

HW MONITOR

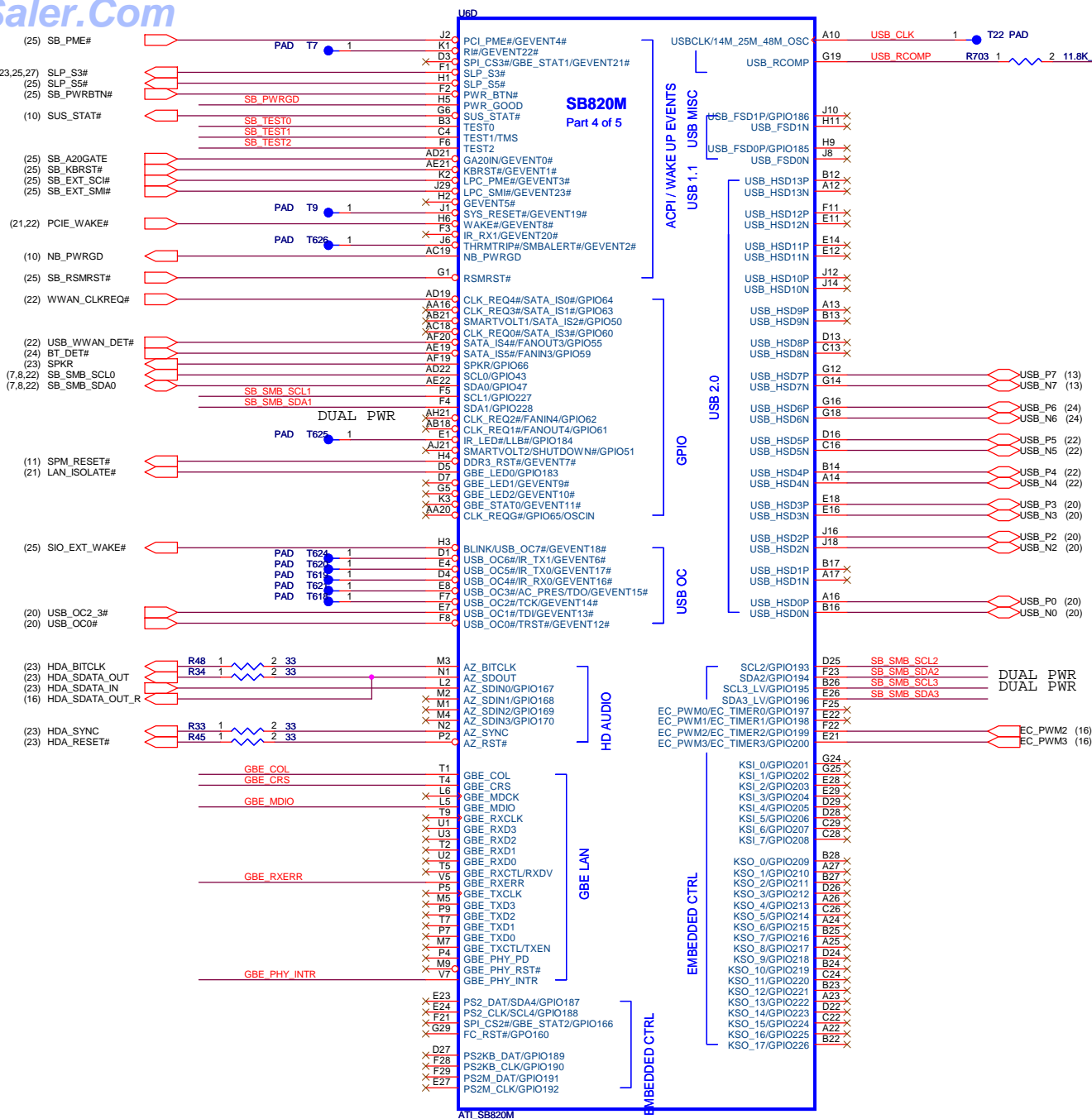
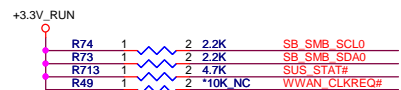
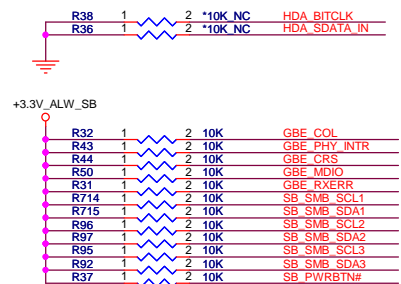
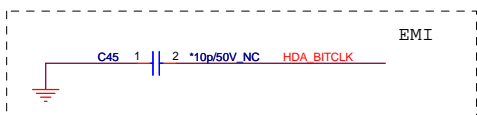
SPI ROM

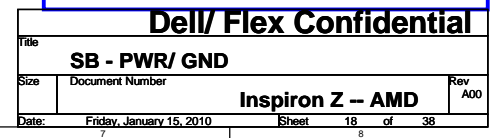
FLASH

SB820M Debug Straps WWW.AliSaler.Com



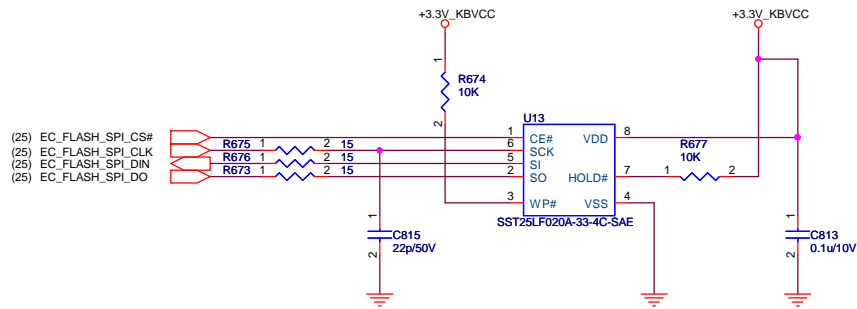
RUN PWR
DUAL PWR



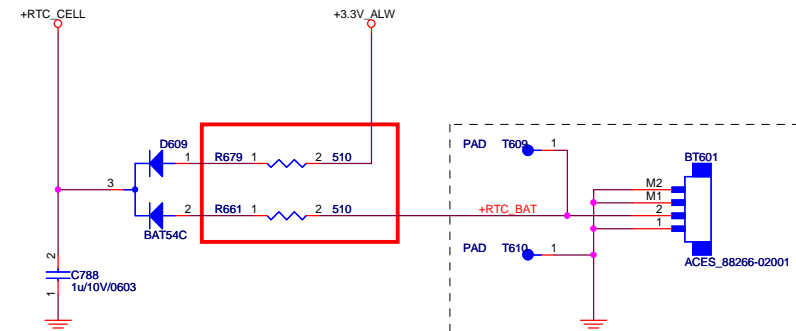


RTC/ SPI

2Mbit (256K Byte), SPI



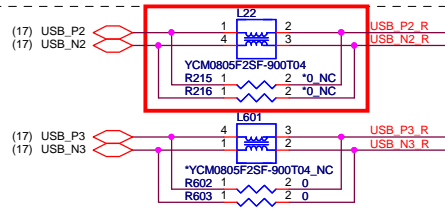
RTC BATTERY



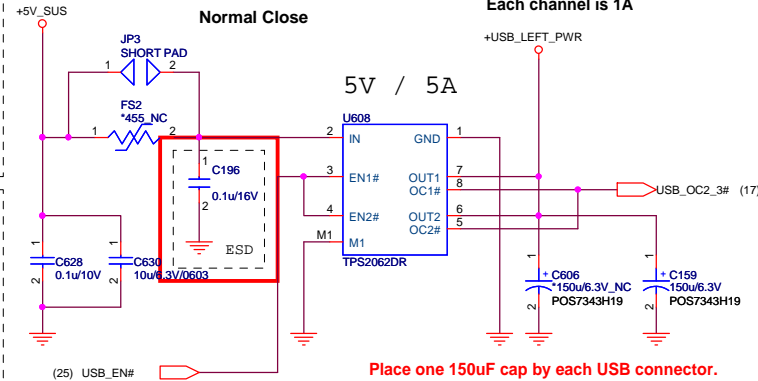
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Title		RTC/ SPI	
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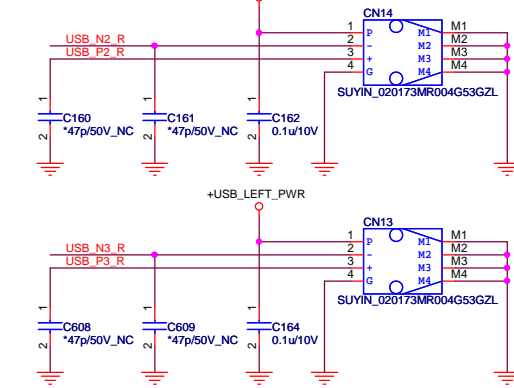
USB Jack x 2



USB POWER SW

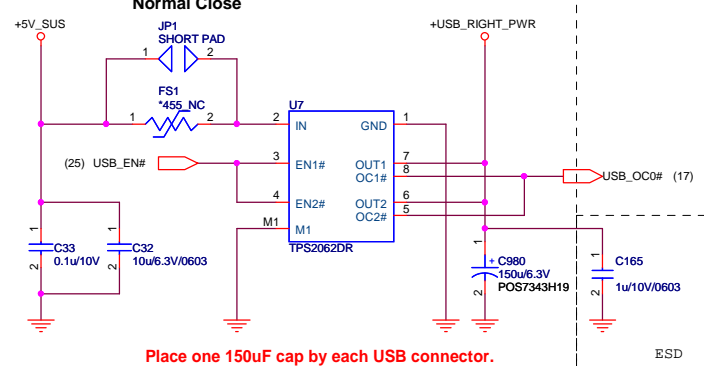


USB CONN

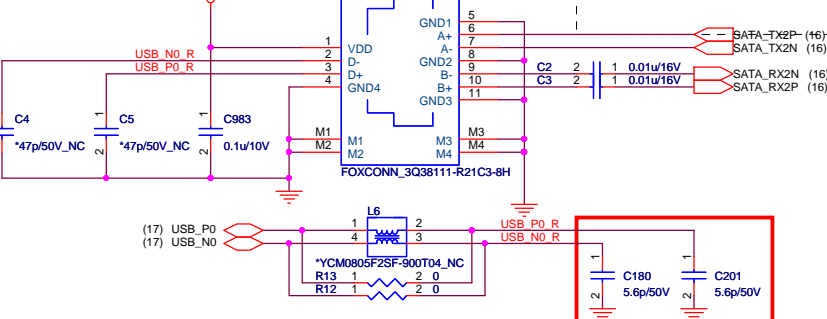


eSATA Connector

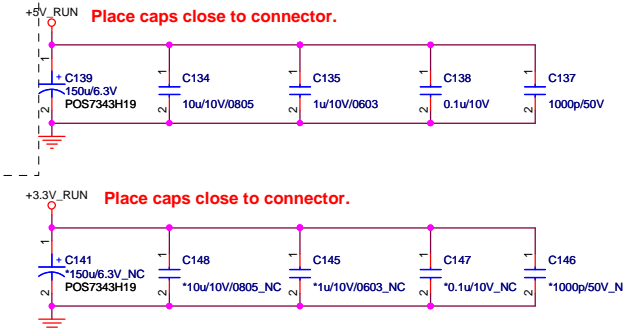
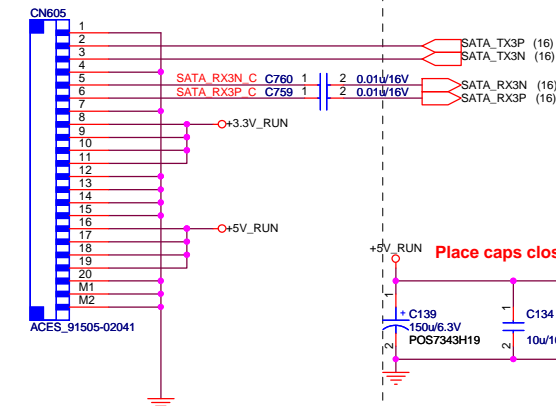
USB POWER SW



ESATA/B CONN



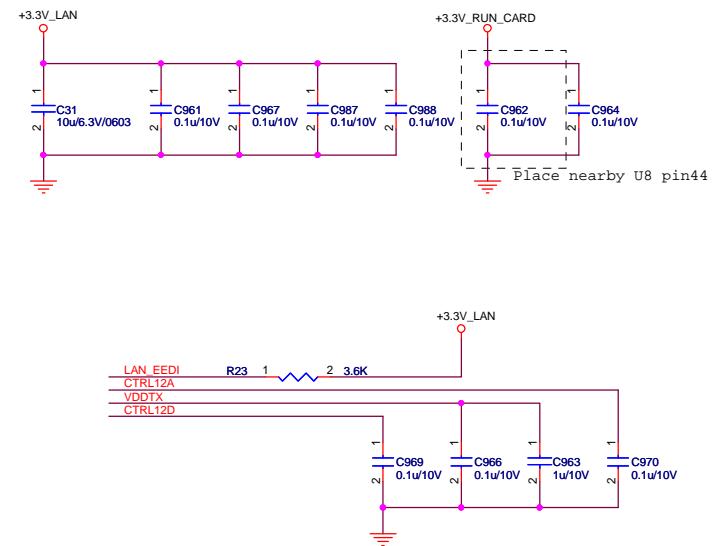
SATA HDD Connector



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USB/ eSATA/ HDD			
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The image shows two wiring diagrams for RJ45 connectors. The top diagram is for the L627 chip, showing connections for RJ45-MDIO+ and RJ45-MDIO- on the left, and RJ45-MDIO+ R, RJ45-MDIO- R, and RJ45-MDIO- R on the right. It includes a yellow chip labeled L627, a yellow chip labeled *YCM0805F2SF-900T04_NC, and resistors R731 and R732. The bottom diagram is for the L5 chip, showing connections for RJ45-MDI1- and RJ45-MDI1+ on the left, and RJ45-MDI1- R, RJ45-MDI1+ R, and RJ45-MDI1+ R on the right. It includes a yellow chip labeled L5, a yellow chip labeled *YCM0805F2SF-900T04_NC, and resistors R2 and R1.

10uF cap is no more than 250mils away from the power pin and have a min trace width of 40mils.

EMI

CON1

SD / MMC

MS

XD

PROCONN_MXPR40-A0-0005

MS CLK

SD CLK

XD WE# SD CD#

XD RE# MS INS#

XD RDY SD WP MS CLK

C172 1 2 5.6p/50V

C38 1 2 5.6p/50V

C35 1 2 *270p/25V NC

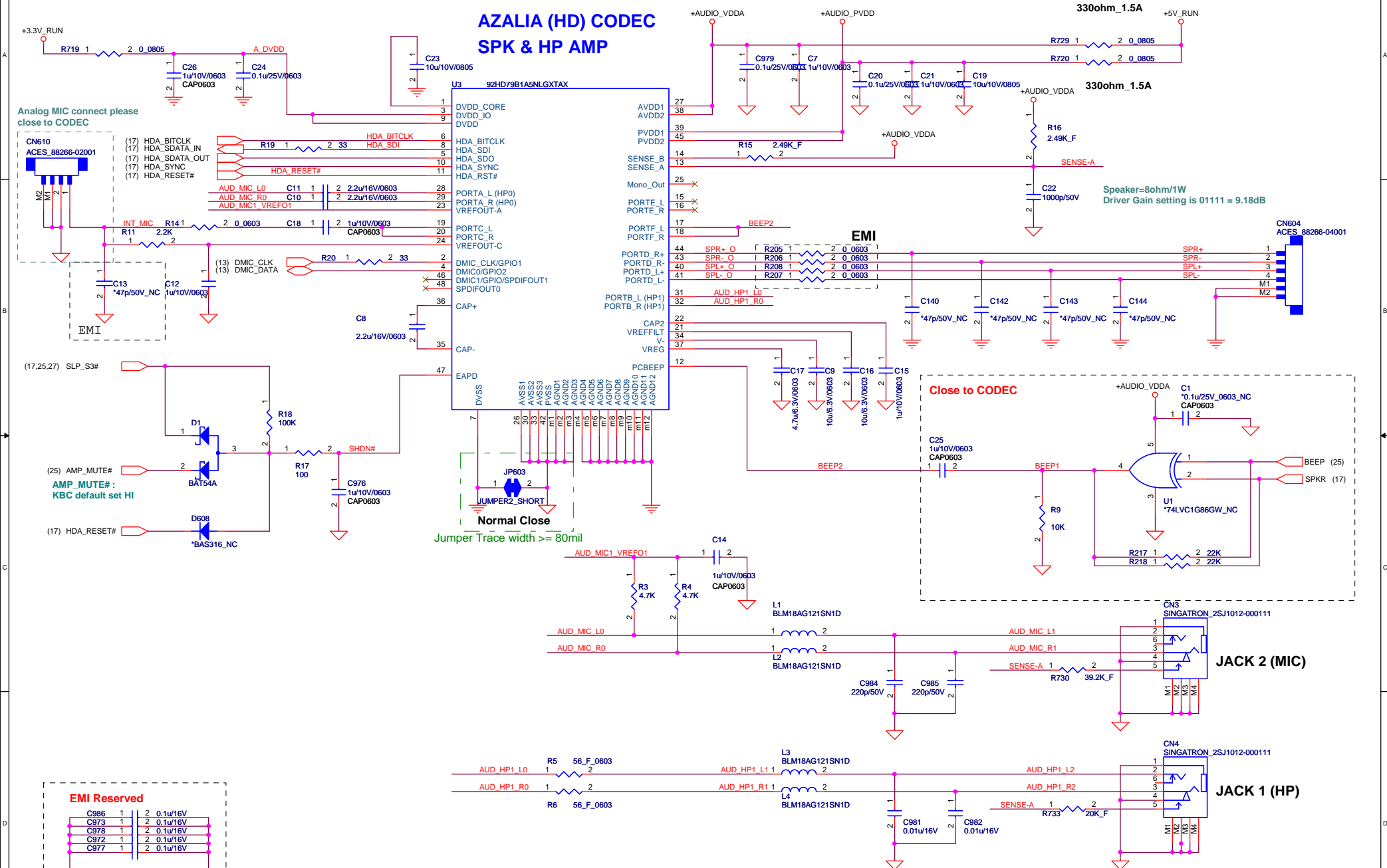
C40 1 2 *270p/25V NC

C36 1 2 *270p/25V NC

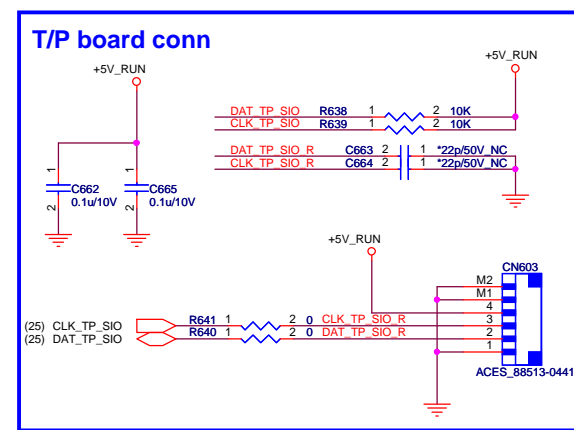
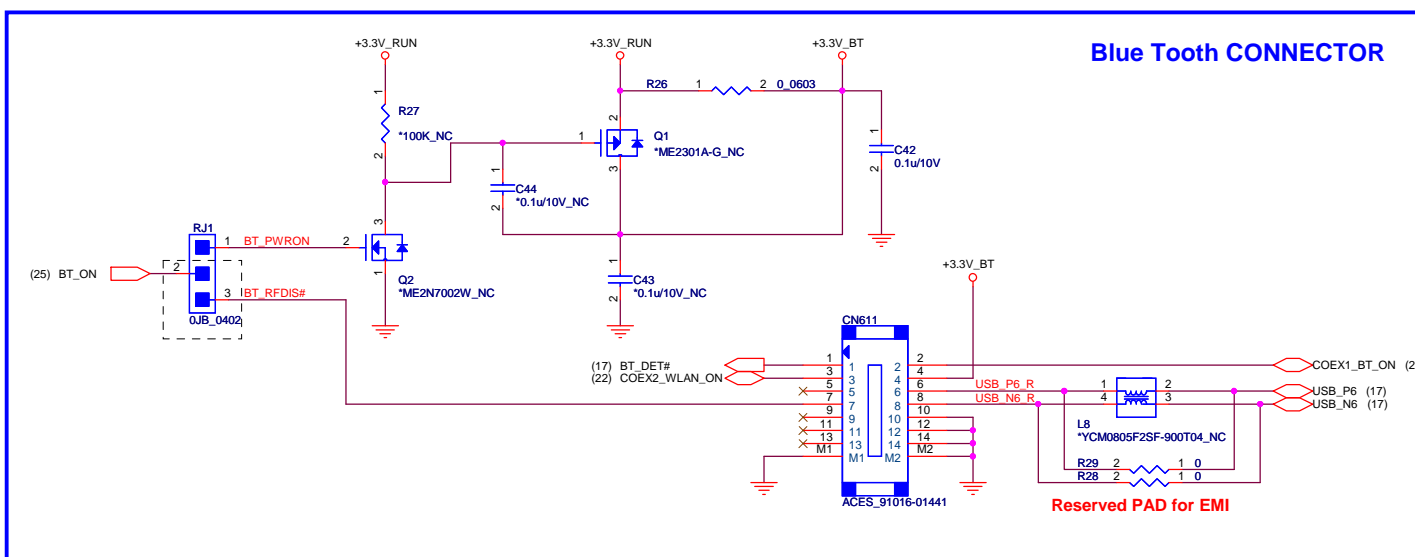
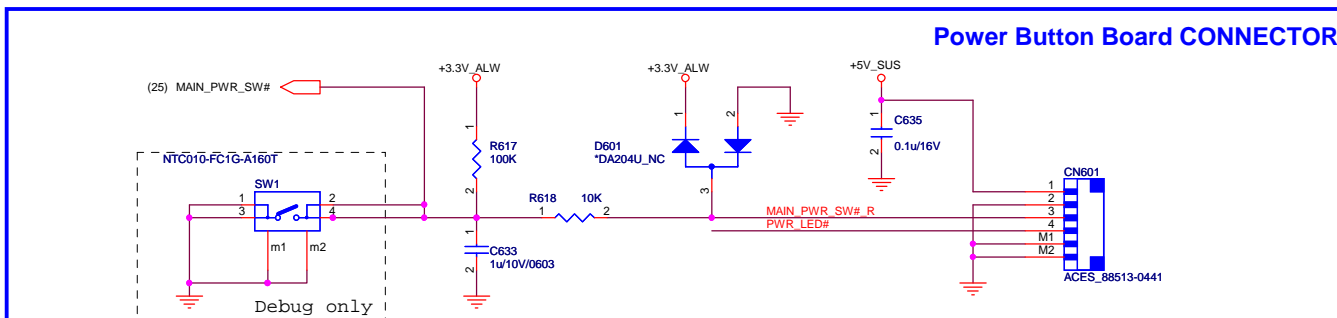
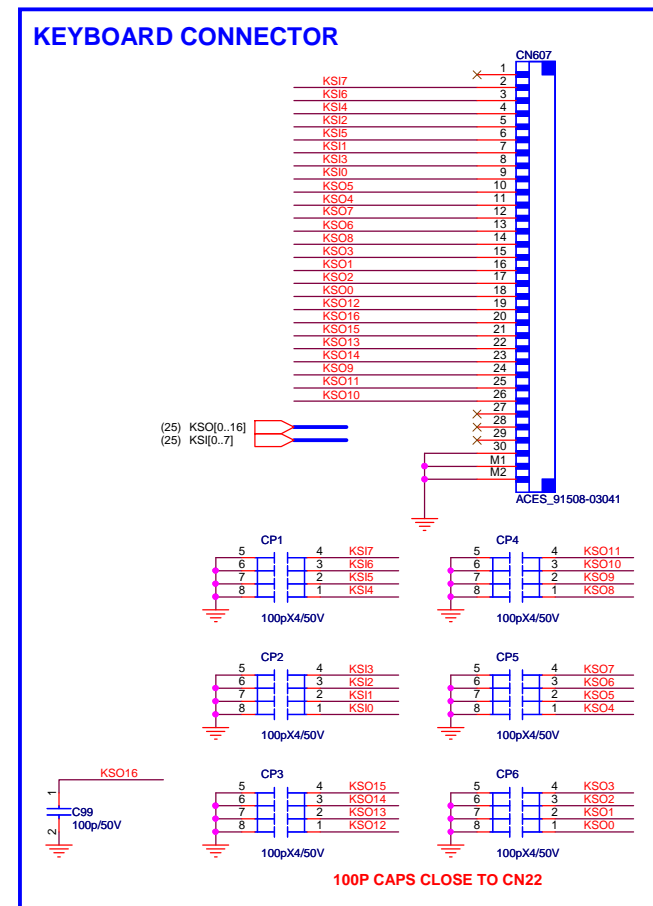
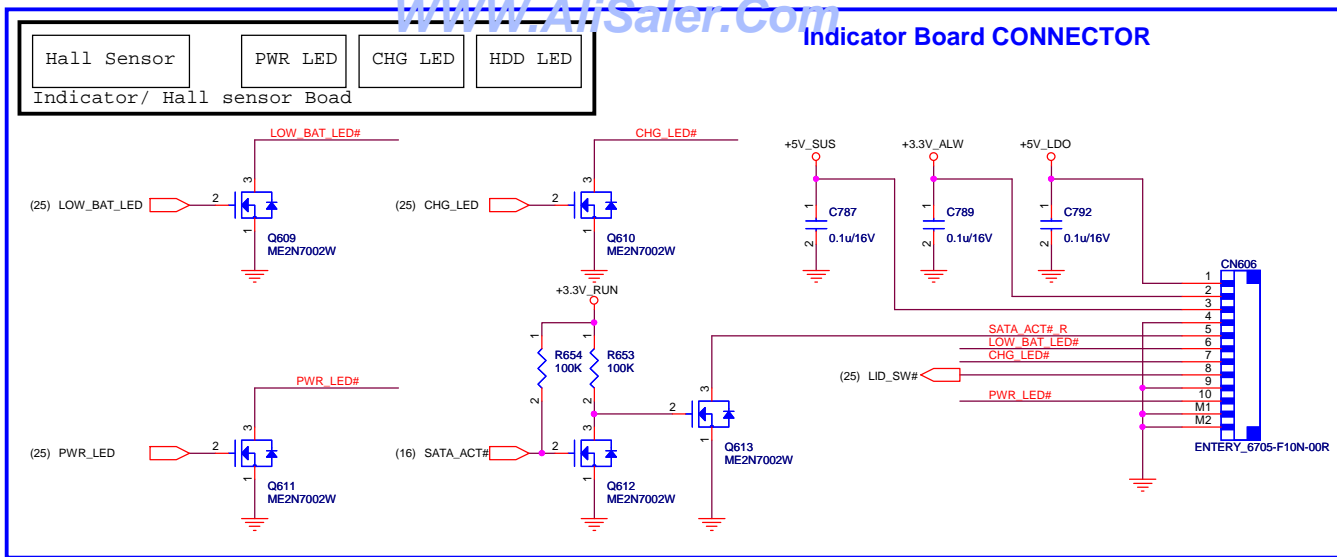
Title			
LAN/ Card Reader -- RL8401			
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(24) KSO[0..16]
(24) KS[0..7]



(28) ADAPT_TRIP_SET

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ITE8502E
LQFP-128L

KEYBOARD

ADC/DAC

PWM

IR/UART

LPC/FWH
FLASH

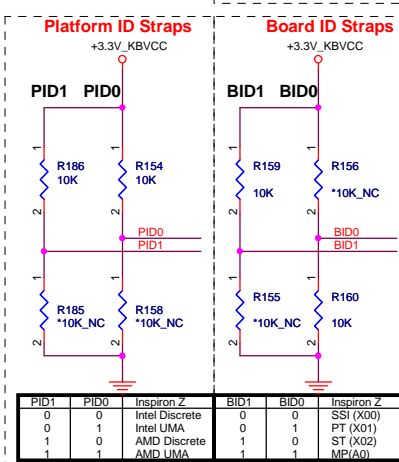
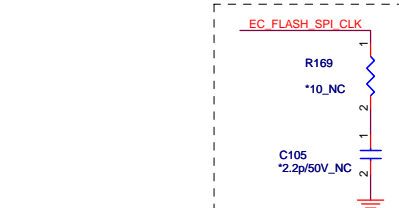
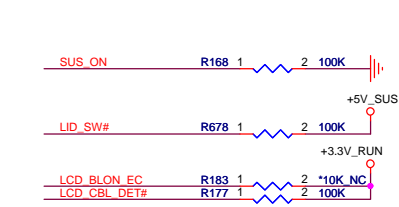
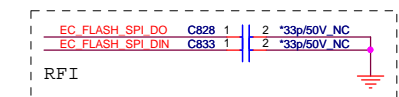
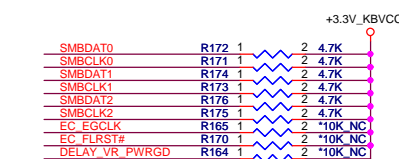
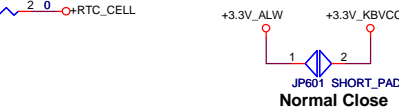
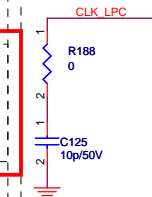
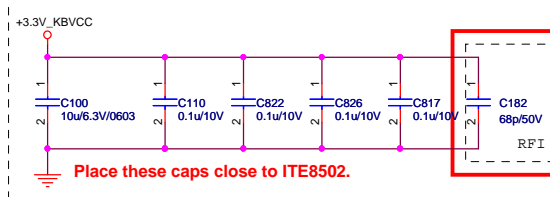
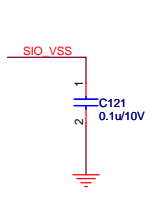
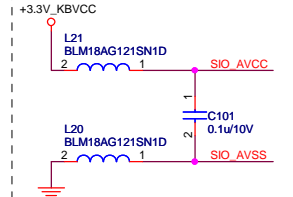
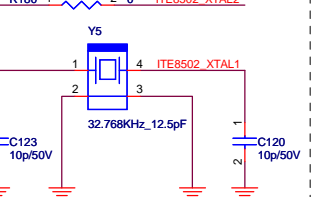
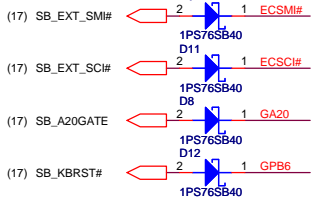
EGPC

PS/2

Charge and BAT

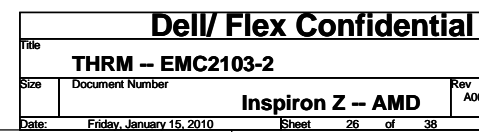
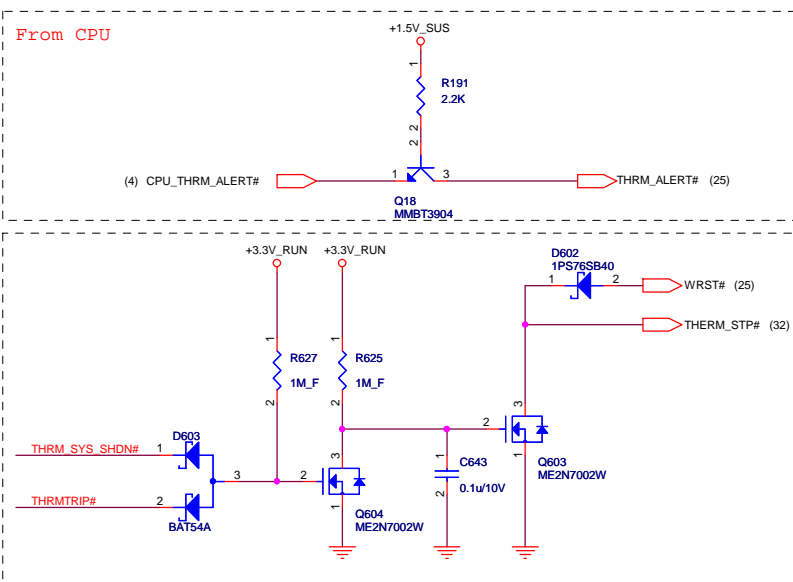
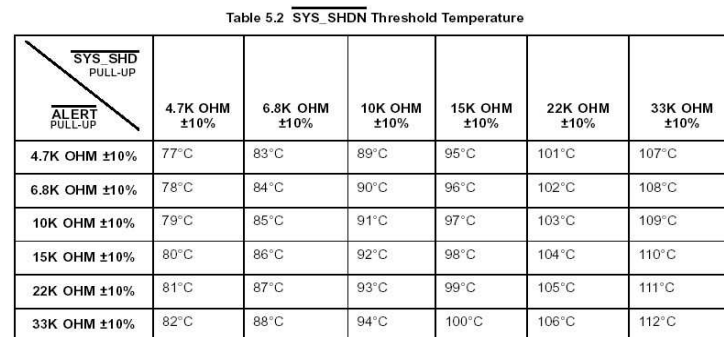
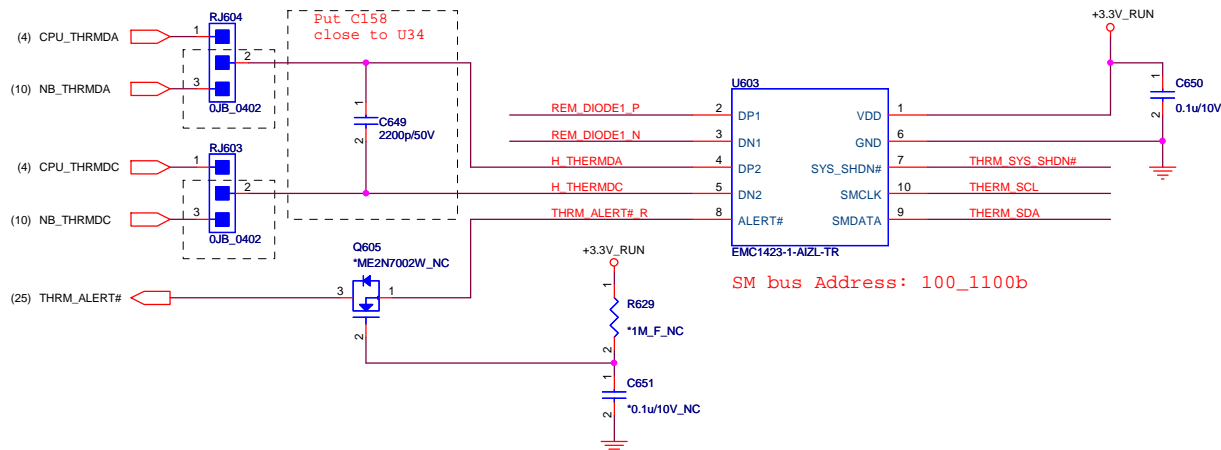
Thermal

CPU TSI



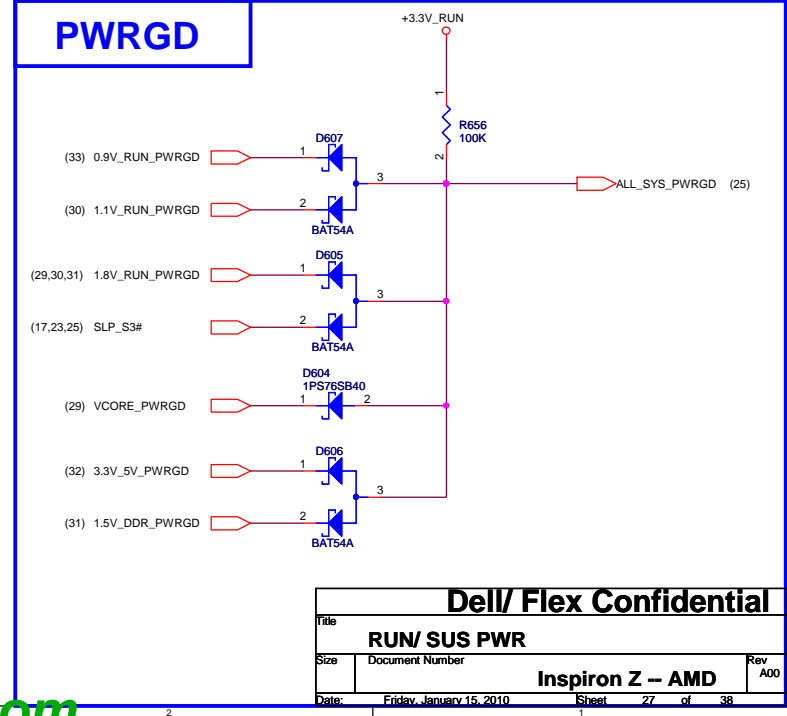
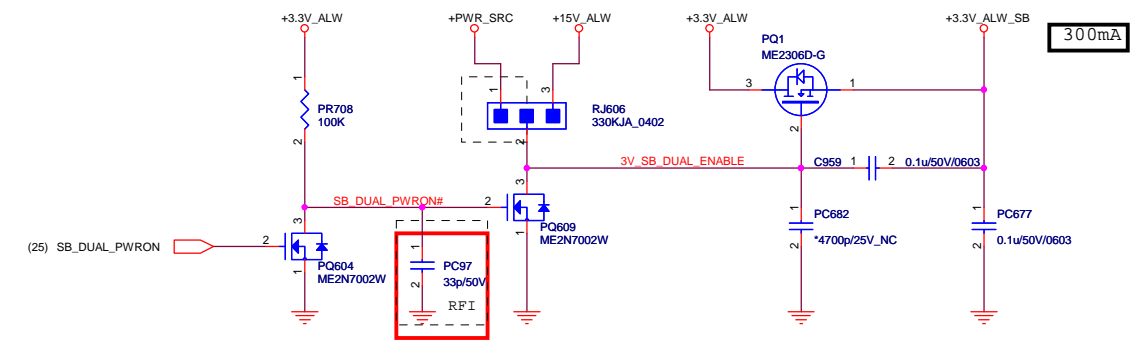
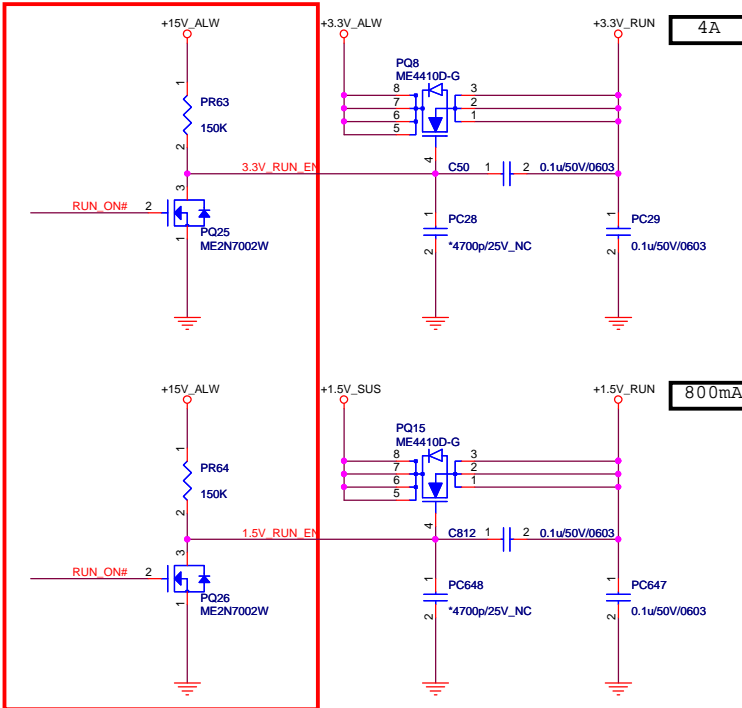
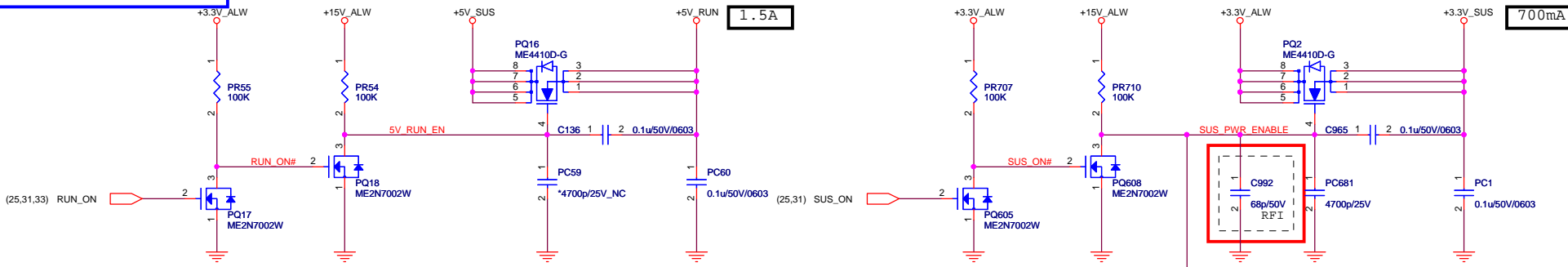
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SIO -- ITE_8502E			
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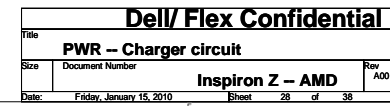


RUN/ SUS CKT

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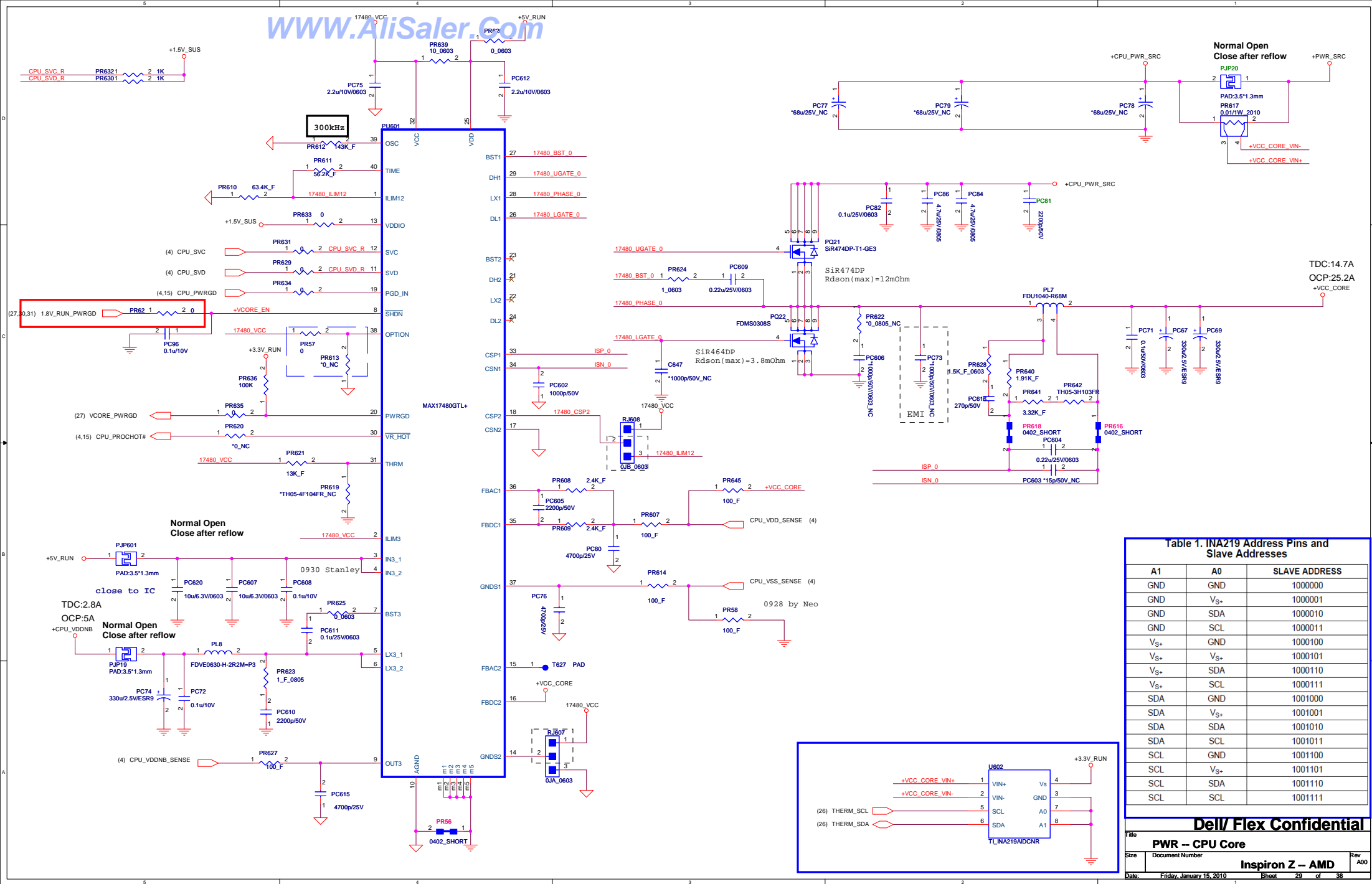


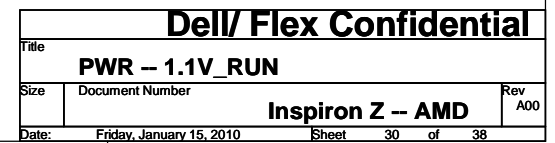
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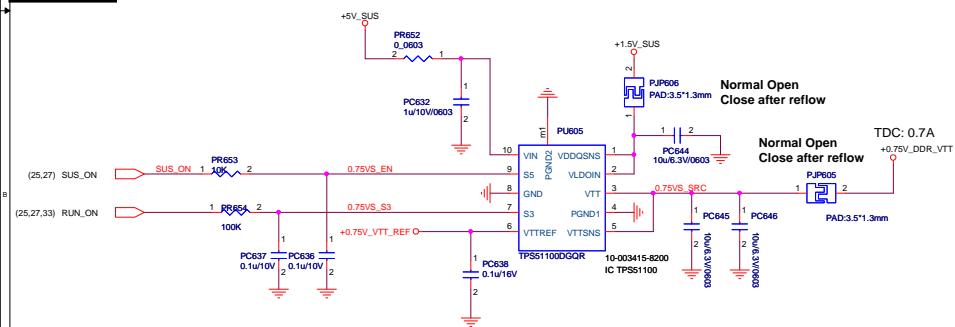
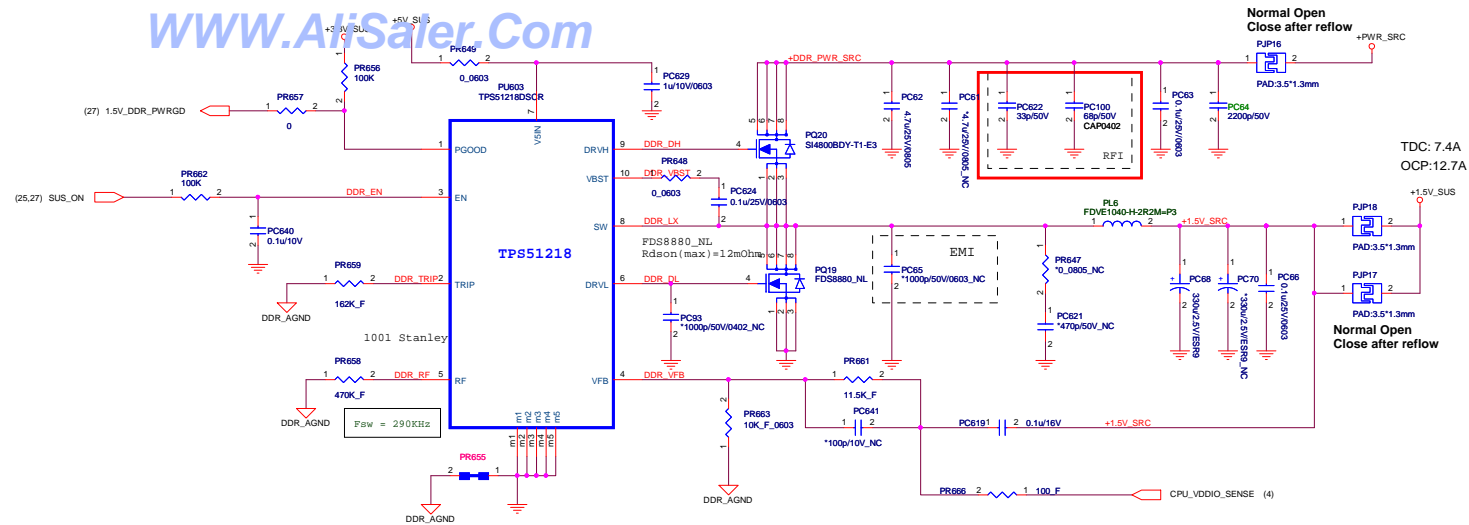


Adapter (W)	Trip current (A)	PQ12	PR37	PR41
65W	3.13	NA	NA	6.49K
90W	4.34	2N7002	19.1K	10K

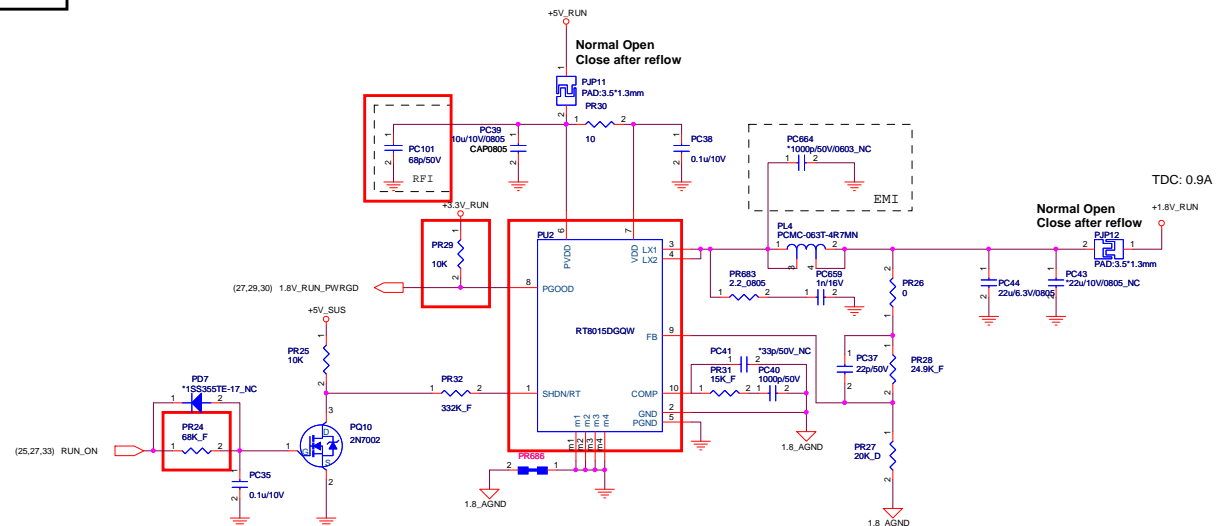
Note 1: PR37 is populated if ADAPT_TRIP_SET is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adapter, grounded for the lower adapter.

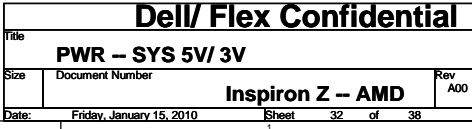






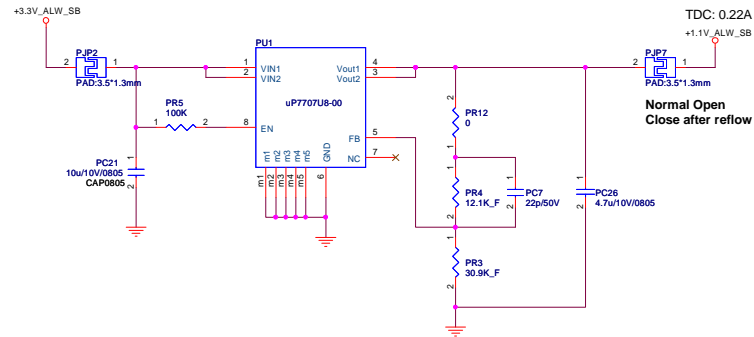
STATE	S3	S5	VTT	VREF
Normal	Hi	Hi	1.25V/0.9V	1.25V/0.9V
Standby	Lo	Hi	12mV/6mV (High-Z)	1.25V/0.9V
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)
Shutdown	Hi	Lo	0V (Discharge)	0V (Discharge)



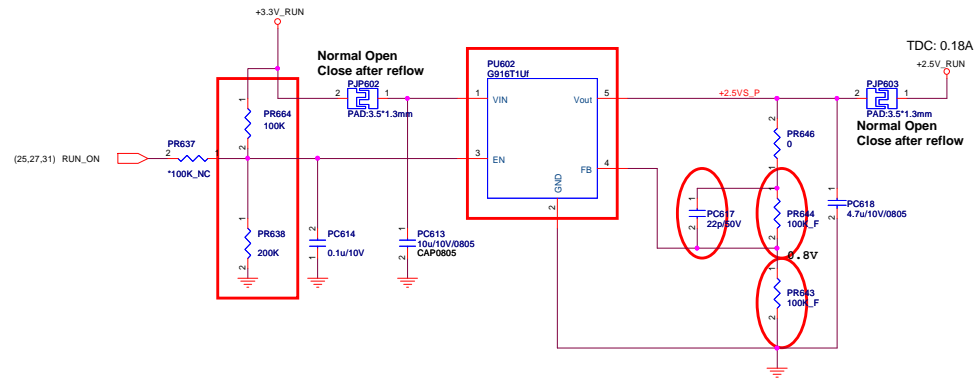


+1.1V_ALW_SB

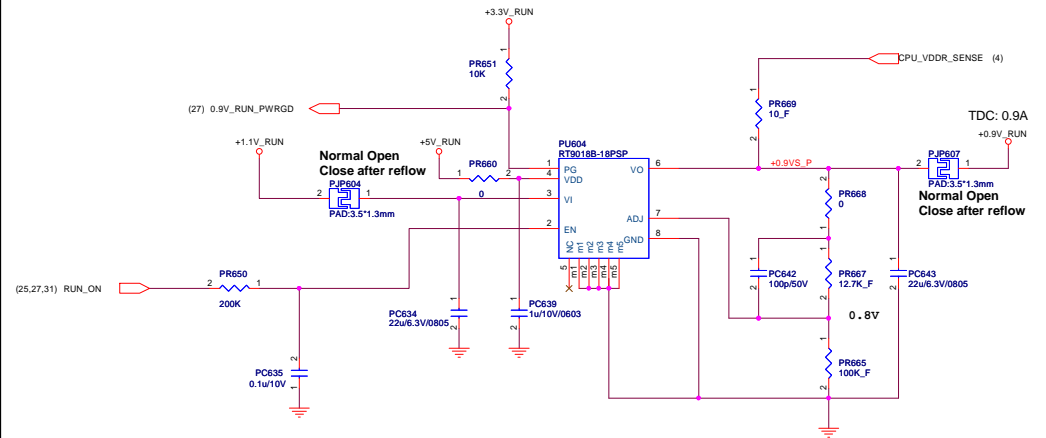
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+2.5V_RUN



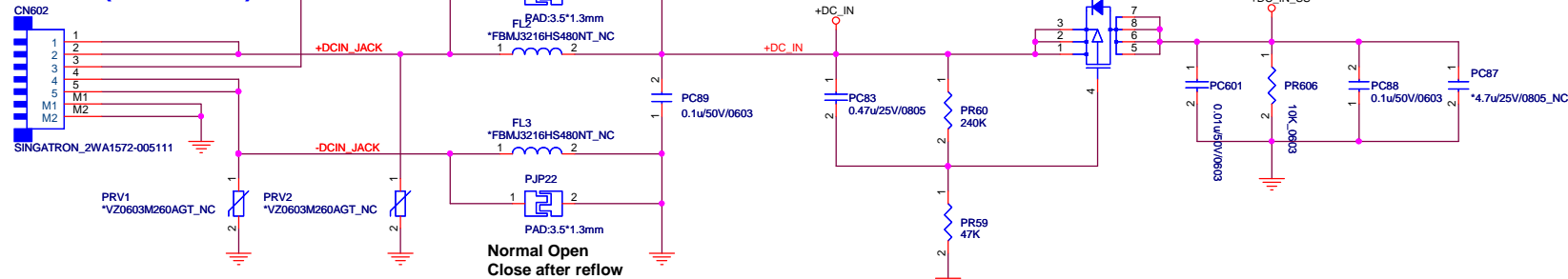
+0.9V_RUN



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File	PWR -- 1.1V_ALW/ 2.5V_RUN/ 0.9V_RUN		
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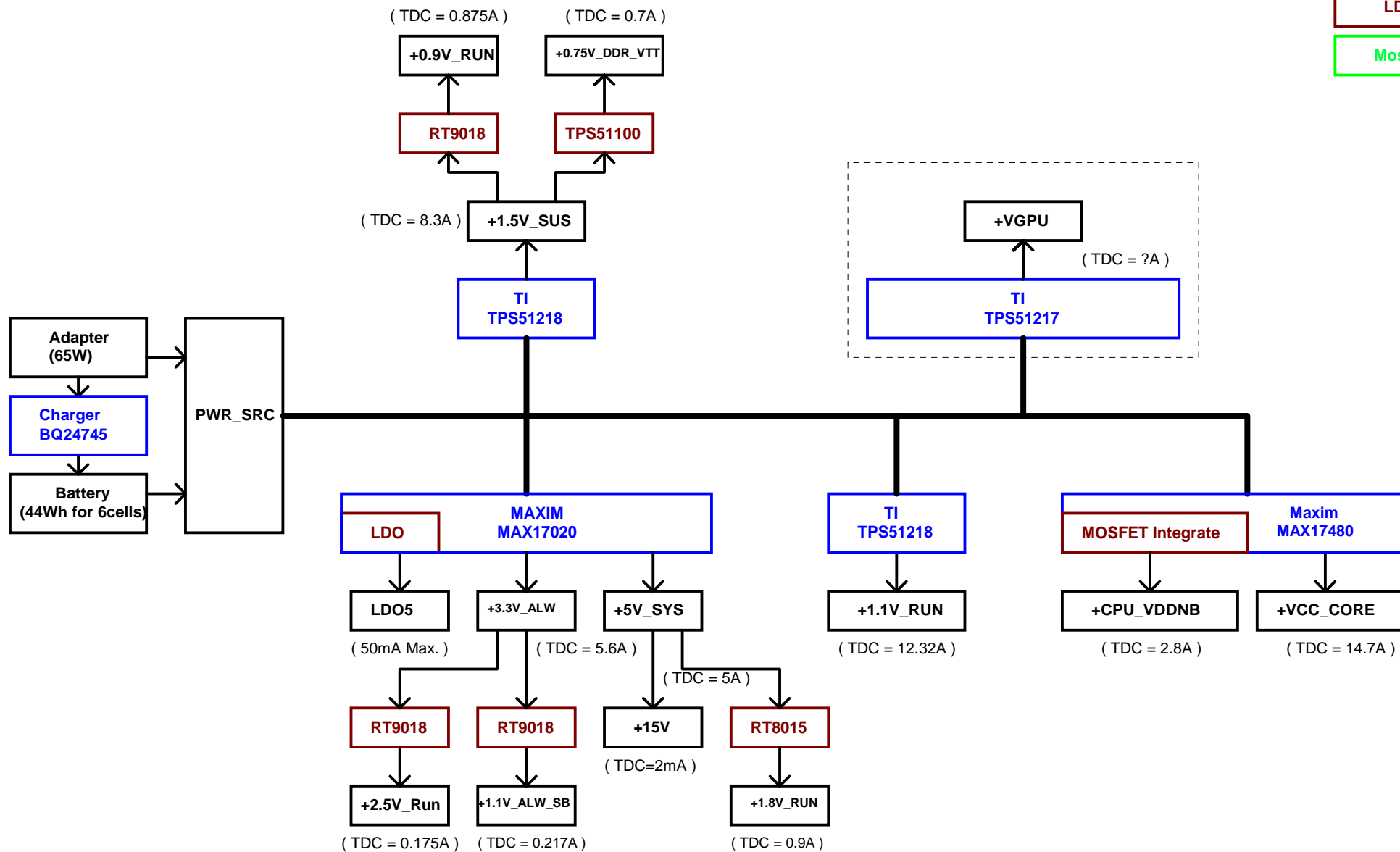
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PWM Switching

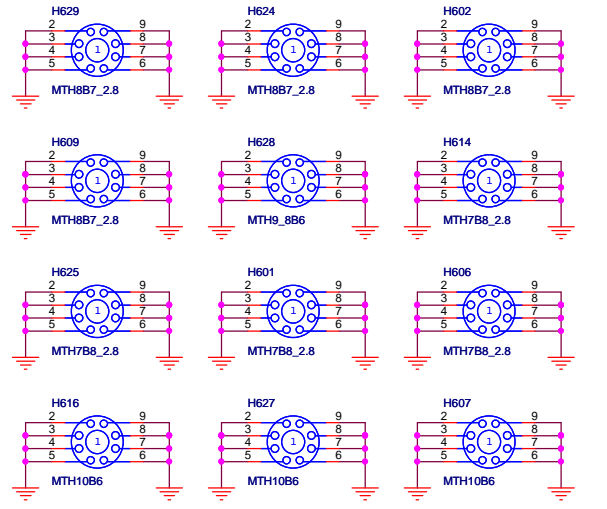
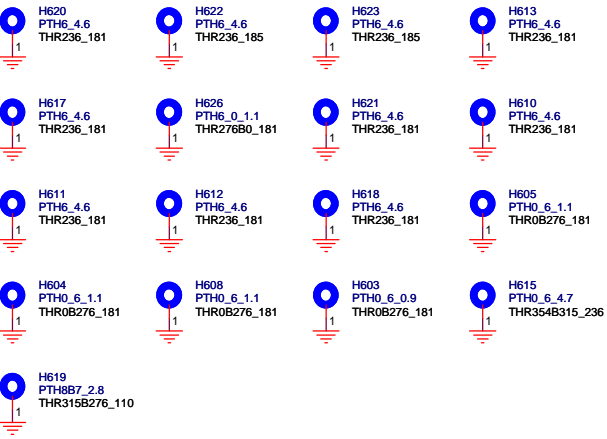
LDO

Mosfet

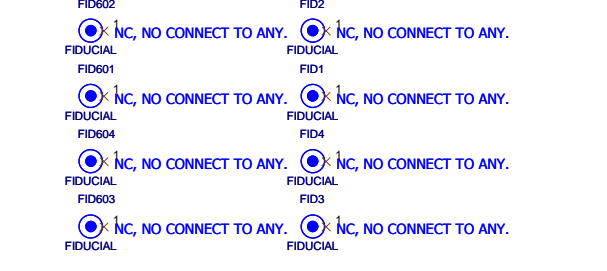


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Cover Sheet			
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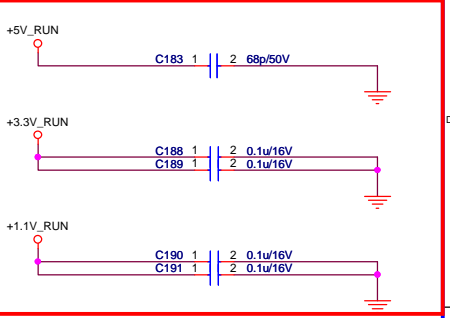
Screw Hole



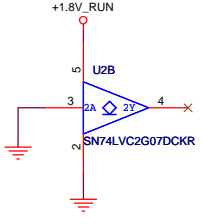
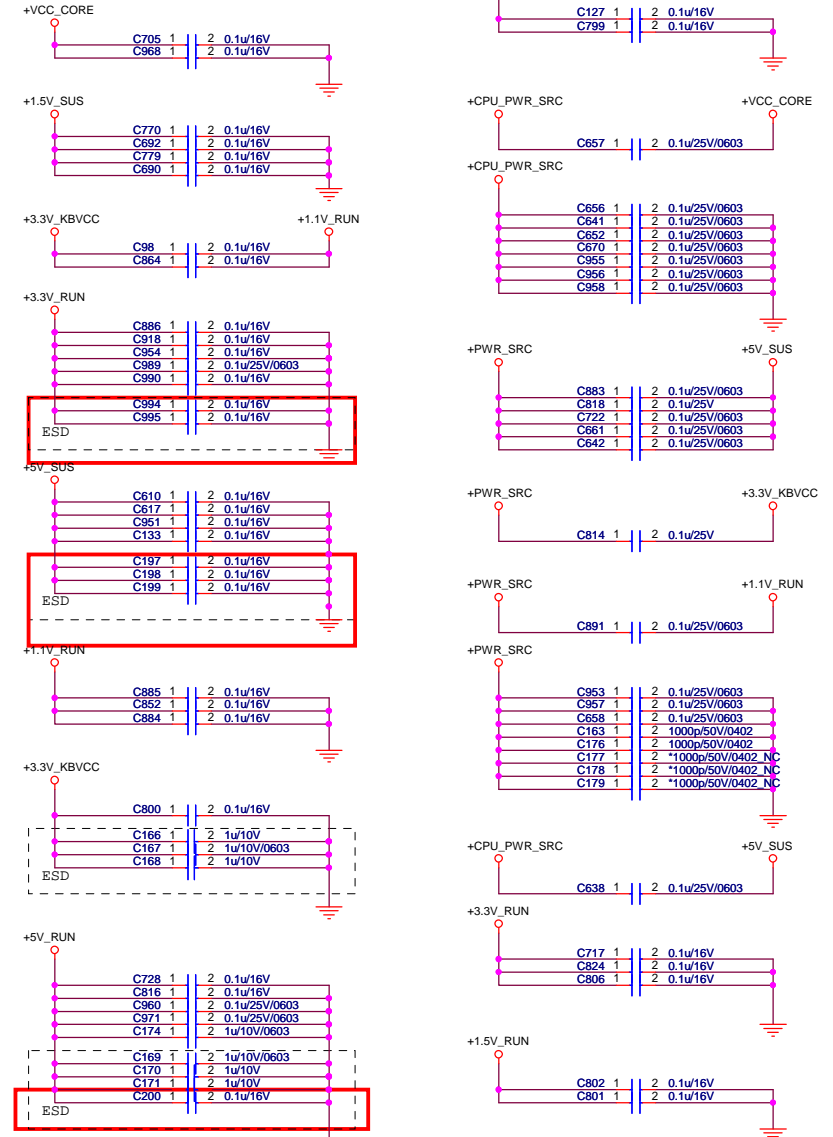
FID



RFI Solution



EMI Solution



Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1			X00		X00 Schematic Official Release	X00	SSI
2	Correct PD601 direction	Correct PD601 direction	X01	34	Horizontally rotate PD601	X01	PT
3	Improve power sequence	Improve power sequence	X01	17, 27, 29	1. Modify D605 pin 2 to "SLP_S3#" 2. Remove PR638 then add PR64& PC96 to enable +VCC_CORE 3. Remove PR709 and add RJ606 to instead on pin 3 also connect "+DC_IN_SS" on RJ606 pin 1. 4. Leave PC59 empty. 5. Add AND gate (U6) combine SLP_S#& SB_PWRGD_EC for SB_PWRGD	X01	PT
4	Modify HDD SATA port to S/B Port3	S/B SATA Port5 wasn't real SATA and AMD recommend us modify to Port 3.	X01	16, 20	Modify HDD SATA port from S/B SATA Port5 to Port3. Also modify net name meet naming rule.	X01	PT
5	Improve RTC battery life cycle	Improve RTC battery life cycle	X01	19	Add D609 to improve RTC battery life cycle	X01	PT
6	Improve X'tal timing	Improve X'tal timing	X01	15, 21	1. Modify C28 to 15pF, C29 to 18pF, C69& C70 to 12pF for 25MHz X'tal. 2. Modify C47& C48 to 22pF for Y5 32.768MHz.	X01	PT
7	MMC card can't be written	MMC card can't be written	X01	21	Modify R24 to 33ohm	X01	PT
8	Solve PC Beep fail	Solve PC Beep fail	X01	23	1. Remove D608, modify R15 to 2.49K_F ohm. 2. Add R217& R218 and leave U1& C1 empty	X01	PT
9	Change FAN Conn Vendor	Request by Thermal Team	X01	26	Modify J601 to ACES 88460-0401	X01	PT
10	Dis-charge LCD VCC	Improve LCD VCC dis-charge timing	X01	13	Add R228& Q19 for LCD VCC dis-charge improvement.	X01	PT
11	Reverse USB I/F of eSATA conn	Keep device direction as the same	X01	20	Modify CN1 (eSATA conn) to FOXCONN 3Q38111-R21C3-8H	X01	PT
12	Modify PCI-E Reset source	AMD recommend to modify	X01	15	Add AND gate for PCI-E Reset timing: 1. SB_PCIE_RST#0& A_RST# for MPCIE_RST#0 2. SB_PCIE_RST#1& A_RST# for MPCIE_RST#1 3. SB_PCIE_RST#2& A_RST# for LAN_RST#	X01	PT
13	TSI function reliability	Make sure TSI I/F workable	X01	4	Modify Q16& Q17 to MMBT3904, add D14, D15, R220& R221 for TSI function.	X01	PT
14	Simplify circuit	Simplify circuit	X01	15	Add R219 and seperate LPC clock for each device.	X01	PT
15	Improve LPC clock	Seperate LPC clock for each device	X01	29	Remove Q601, Q602, R624& R628 to simplify SM Bus 1	X01	PT
16	Prevent leakage current from external device	Prevent leakage current from external device	X01	14	Add D16, D17 to prevent leakage current from external device.	X01	PT
17	Single Phase Core VR configuration	Single Phase Core VR configuration	X01	29	1. Add RJ607 2. FBDC2 connected to +VCC_CORE 3. FBAC2 add T627 4. Add RJ608	X01	PT
	Low side MOS induce	Low side MOS induce	X01	30, 31	1. Modify to FDMS0308s 2. Add PC93 for 1000pF_0402/ NA 3. Add PC94, PC95 for 1000pF_0402 Add PC92 1000pF NA		
	Avoid Low Side MOS induce	Avoid Low Side MOS induce	X01	30			
	High Side MOS Vds ring over spec.	Add Snuber on Low Side Vds	X01	30	PR670 Mounted 1ohm, PC649 Mounted 680pF		
	OC Protection	OC Protection	X01	31, 32	1. PR659 modify to 120K 2. PR19 modify to 301K		
	Input ripple over spec.	Input ripple over spec.	X01	31, 33	1. PC634, PC644 modify to 10uF/6.3V 2. Add C163, C176~ C179.		
	Modify package of capacity	ME height limitation	X02	29	Modify PC607 to 0603 package		

History - 1

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Rev A00

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Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
18	Seperate RF control signal	Seperate RF control signal (Dell)	X01	22, 24, 25	1. Modify U11 (EC) pin 85, 87, 88 as BT_ON, WLAN_RF_DIS#, WWAN_RF_DIS#. 2. Move CAM_PWR_ON# to U11 pin 94.	X01	PT
19	ESD SSI solution	ESD SSI solution	X01	20, 36	Add C165~ C171 for ESD solution	X01	PT
20	LAN signal swap	For layout concern	X01	21	Swap LAN_MDI1#& LAN_MDIN, 1RJ45-MDI1+& RJ45-MDI1-.	X01	PT
21	Add Test Pad for USB CLK	AMD recommend	X01	17	Add Test Pad T22 by AMD recommend	X01	PT
22	Modify RAM Vref source	Modify RAM Vref source	X01	4, 7, 8	1. R635, R636, C654, C655, R652, R651, C758& C763 Mounted 2. Leave R648, R634 empty.	X01	PT
23	Setting GPIO level	Prevent GPIO pin floating	X01	15, 17	Add R222, R223, R734, R735, R49	X01	PT
24	Modify SPI ROM to 2M + 256K	Modify SPI ROM to 2M + 256K	X01	16, 19	Modify U9 to 2M bytes and U13 to 256K bytes.	X01	PT
25	Keeping LAN PWR source clear	Keeping LAN PWR source clear	X01	21	Delete C971& C968 and add C987, C988	X01	PT
26	Keeping EC pin level	Keeping EC pin level	X01	25	Leave R165, R170, R167, R164 empty	X01	PT
27	RFI solution (SSI)	RFI solution (SSI)	X01	25, 31	Mounte C836 and add PC622 fro 33pF	X01	PT
28	EMI solution (SSI)	EMI solution (SSI)	X01	13, 14, 21, 24, 26, 36	1. Modify L625, L10, L11, L12, L13, L5, L627 to YCM0805F2SF-900T 2. Modify R25 to 33ohm, mounte C38 and add C172 for 10pF 3. Mounte CP1, CP2, CP3, CP4, CP5, CP6& C99 4. Add C173& C175 on FAN signal 5. Add C968, C990, C989, C174, C670, C955, C956& C958	X01	PT
29			X01		X01 Schematic Official Release	X01	PT
30	Remove unused parts	Remove unused parts	X02	16, 25	Remove R140, R141, R142& R143	X02	ST
31	Prevent leakage current	Prevent leakage current	X02	16	Modify U9 power and pull-high power to +3.3V_ALW_SB	X02	ST
32	Seperate LPC CLK	Improve LPC CLK waveform	X02	15	Connecotor R219.1 to U6.H25 (LPC_CLK1).	X02	ST
33	HTC IPCC function improve	Implement IPCC function	X02	4, 25	Add Q616 and add U11.104 as "IPCC_SMI#" for IPCC function	X02	ST
34	Fine tune PWR sequence	Fine tune PWR sequence	X02	27, 29, 30, 31	1. Seperate "RUN_PWER_ENABLE" and add PR63, PR64, PQ25& PQ26. 2. Modify PR62, PR53 to 0ohm, PR24 to 68Kohm and PR29 to 10Kohm. 3. Modify VCORE& +1.1V_RUN enable signal to "1.8V_RUN_PWRGD" 4. Add PR664 for enable of +2.5V_RUN.	X02	ST
35	EMI solution (PT)	EMI solution (PT)	X02	20, 21	1. Modify L22 from N.A to mounted 2. Modify C38, C172 from 10 pF to 5.6pF.	X02	ST
36	RFI solution (PT)	RFI solution (PT)	X02	6, 10, 13, 15, 18, 27, 28, 30, 31, 36	1. Add C102, C181, C993, PC622 for 33pF 2. Add C183, C184, C185, C991, C992, PC98, PC99, PC100, PC101, PC102, PC683 for 68pF 3. Add PC103 for 1uF 4. Add C186, C187 for 0.1uF_0603 5. Add C188, C189, C190, C191, C192, C193, C194, C195 for 0.1uF 6. Add PC104 for 2200pF 7. Delete C834, C836 and add R224 as damping resistor of "EC_FLASH_SPI_CLK"	X02	ST
37	Safety solution (PT)	Improve Safety	X02	19	Add R679 and modify R661 to D609.2	X02	ST
38	ESD solution (PT)	ESD solution (PT)	X02	20, 36	Add C196, C197, C198, C199, C200, C994, C995 for ESD solution.	X02	ST
39	eSATA USB signal improve (AMD)	eSATA USB HS eye diagram improve	X02	20	Add C180, C201 by 5.6pF for eSATA USB signal improvement.	X02	ST

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